Memory Address Decoding

ROAD MAP

- **Memory Address Decoding**
- **S-RAM Interfacing Process**
- **Solved Examples For S-RAM Decoding**
- **D-RAM Interfacing**

Memory Addressing

- The processor can usually address a memory space that is much larger than the memory space covered by an individual memory chip. In order to splice a memory device into the address space of the processor, decoding is necessary. For example, the 8088 issues 20-bit addresses for a total of

- **1MB** of memory address space. However, the BIOS on a 2716 EPROM has only 2KB of memory and 11 address pins. A decoder can be used to decode the additional 9 address pins and allow the EPROM to be placed in **any** 2KB section of the 1MB address space.

Memory Address Decoding

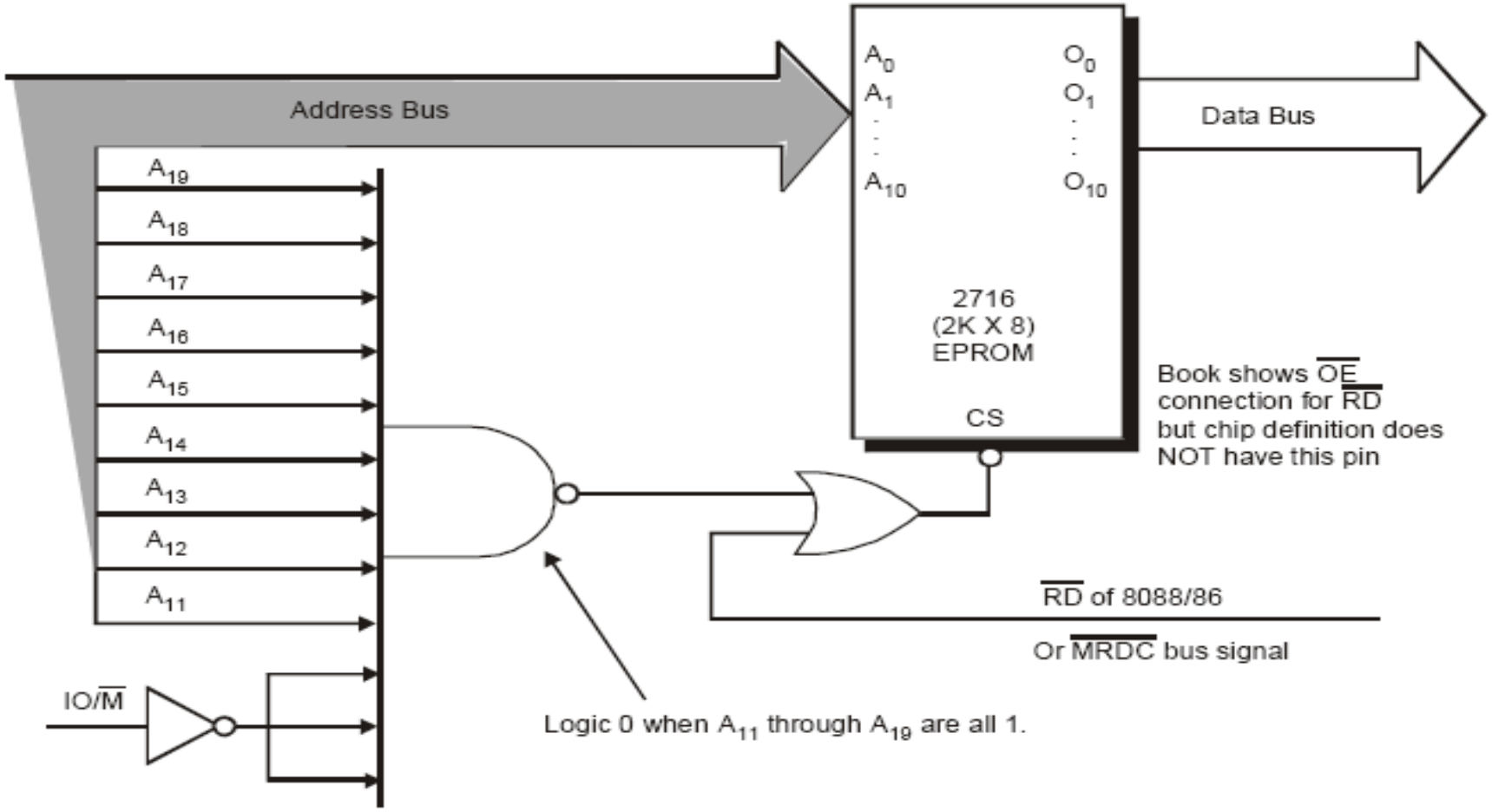


Fig. 5.48. Memory address decoding.

Semiconductor Memory Interfacing

- **S-RAM Interfacing.** Semiconductor RAMs are basically classified into 2 categories
- (a) Static RAM or (S-RAM)
- (b) Dynamic RAM or (D-RAM)
- Here we will consider the interfacing of static RAM and ROM with 8086 microprocessor.

Interfacing Process

- The semiconductor memories are organized as two dimensional arrays of memory locations, for example 2K X 8 or 2K byte memory or 4K X 8 , 4K byte memory which contains 4096 locations, where each location contains 8-bit data. Only one f the 4096 locations can be selected at a time.
- In general, to address a memory location out of 'N' memory locations, one would require at least 'n' bits of address i.e. 'n' address lines where $n = \log_2 N$.
- Hence if the microprocessor has 'n' address lines, then it is able to address at most N locations of memory where $\boxed{2^n = N}$

- If out of N locations only 'P' primary locations are to be interfaced, then the least significant 'P' address lines out of the available 'n' lines can be directly connected from the microprocessor 8086 to the memory chip while the remaining (n – p) higher order address lines may be used for address decoding.
- The output of the decoding circuit is connected with the C S pin of the memory chip.

- **The procedure of interfacing S-RAM with 8086 microprocessor is as given below :**

(1) Arrange the available memory chips so as to obtain 16-bit data bus width. The upper 8-bit bank is called as the "odd address memory bank" and the lower 8-bit bank is referred to as the "even address memory bank".

(2) Now one must connect the available memory address lines of memory chips with those of the 8086 microprocessor and connect the memory RD and WR inputs to the corresponding processor control signals.

(3) Connection of the 16-bit data bus of the memory bank with that of the microprocessor 8086must be done.

(4) BHE , A0 and the rest of the address lines left are used for decoding the required chip select signals for the odd and even memory banks.

Solved Problems

- **Example 5.1. Interface two 4K X 8 EPROMS and two 4K X 8 RAM chips with 8086, microprocessor and draw the suitable circuit showing their interfacing ?**

- **Solution.** The address of the RAM may be selected anywhere in the 1 MB address space of 8086, but to make the address space continuous we would follow the given procedure. After reset the IP and CS are initialized to for address FFFF0H. We must first calculate the total number of address lines required for 8K bytes of EPROM which is 13, as we have seen earlier that we have $N = 2n$ hence we get

$$2^{13} = 8K$$

Decoded Map

- Address lines A13-A19 are used for decoding to generate the chip select. The BHE signal goes low when a transfer is at odd address or higher byte of data is to be accessed.

Memory Map

Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
FFFFFH	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
EPROM ADDRESS					4K X 8															
FFFFFH	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
FFFFFH	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
RAM ADDRESS					4K X 8															
FCOOOH	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- The memory system here contains in total four 4K X 8 memory chips. The two 4K X 8 chips of RAM and ROM are arranged in parallel to obtain 16-bit data bus width. If A0 is 0 i.e. the address is even and is in RAM, then the lower RAM chip is selected indicating 8-bit transfer at an even address.
- If A0 is 1, i.e. the address is odd and is in RAM the BHE goes low, the upper RAM chip is selected, further indicating that the 8-bit transfer is at an odd address. If the selected addresses are in ROM, the respective ROM chips are selected. If at a time A0 and BHE both are 0, both the RM or ROM chips are selected i.e. the data transfer is of 16-bits.

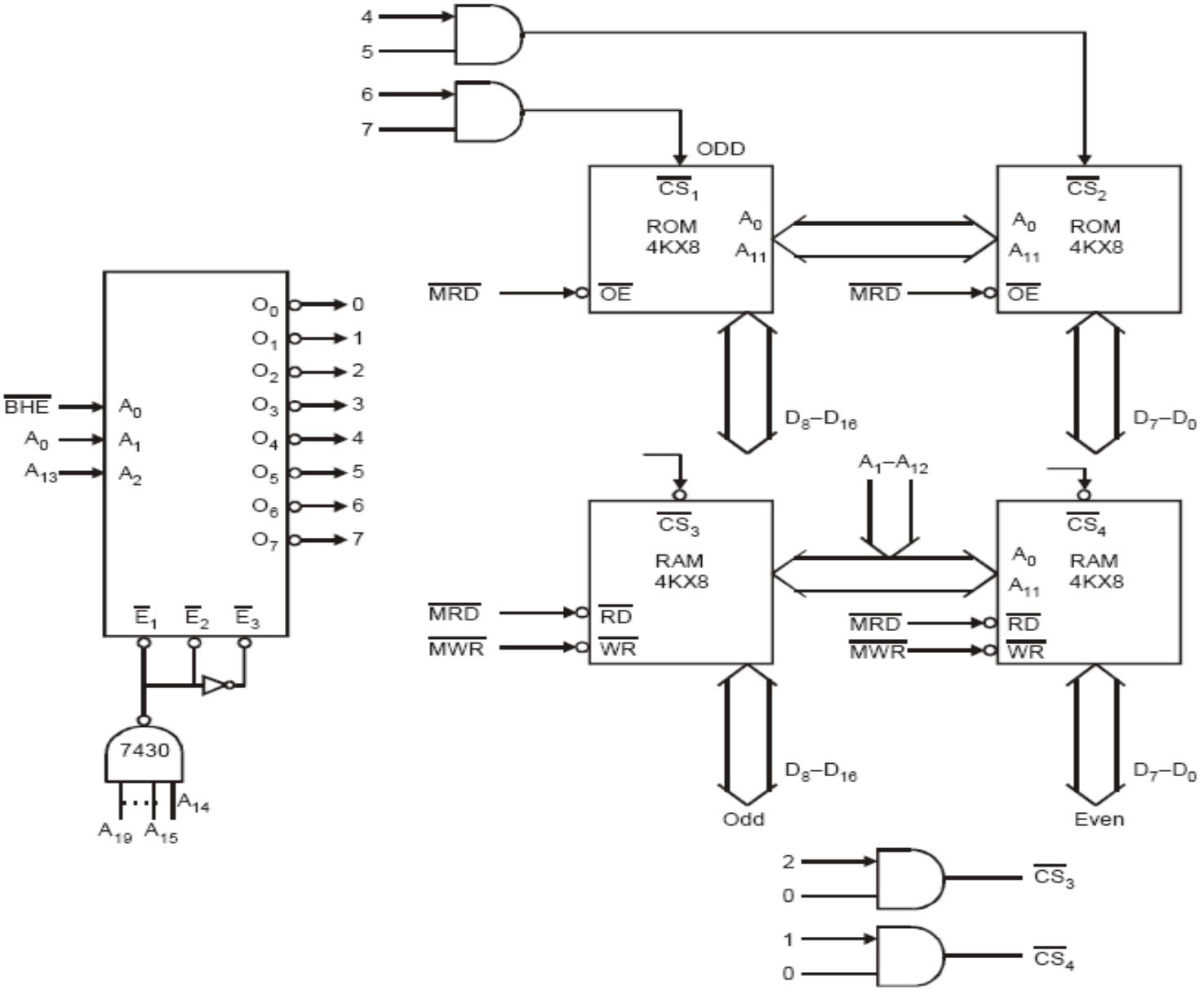


Fig. 5.52. Interfacing circuit.

- **Example 5.2. Design an interface between CPU 8086 and two chips of 32K X 8 ROM and four chips of 32 K X 8 RAM according to the following memory map ?**

ROM 1 and ROM 2 ⇒ F0000H–FFFFFH

RAM 1 and RAM 2 ⇒ D0000H–DFFFFH

RAM 3 and RAM 4 ⇒ E0000H–EFFFFH

Solution. **Address Map**

Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
FOOOOH	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ROM 1 and ROM 2																				
FFFFFH	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DOOOOH	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RAM 1 and RAM 2																				
DFFFFH	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
EOOOOH	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RAM 3 and 4																				
EFFFFH	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

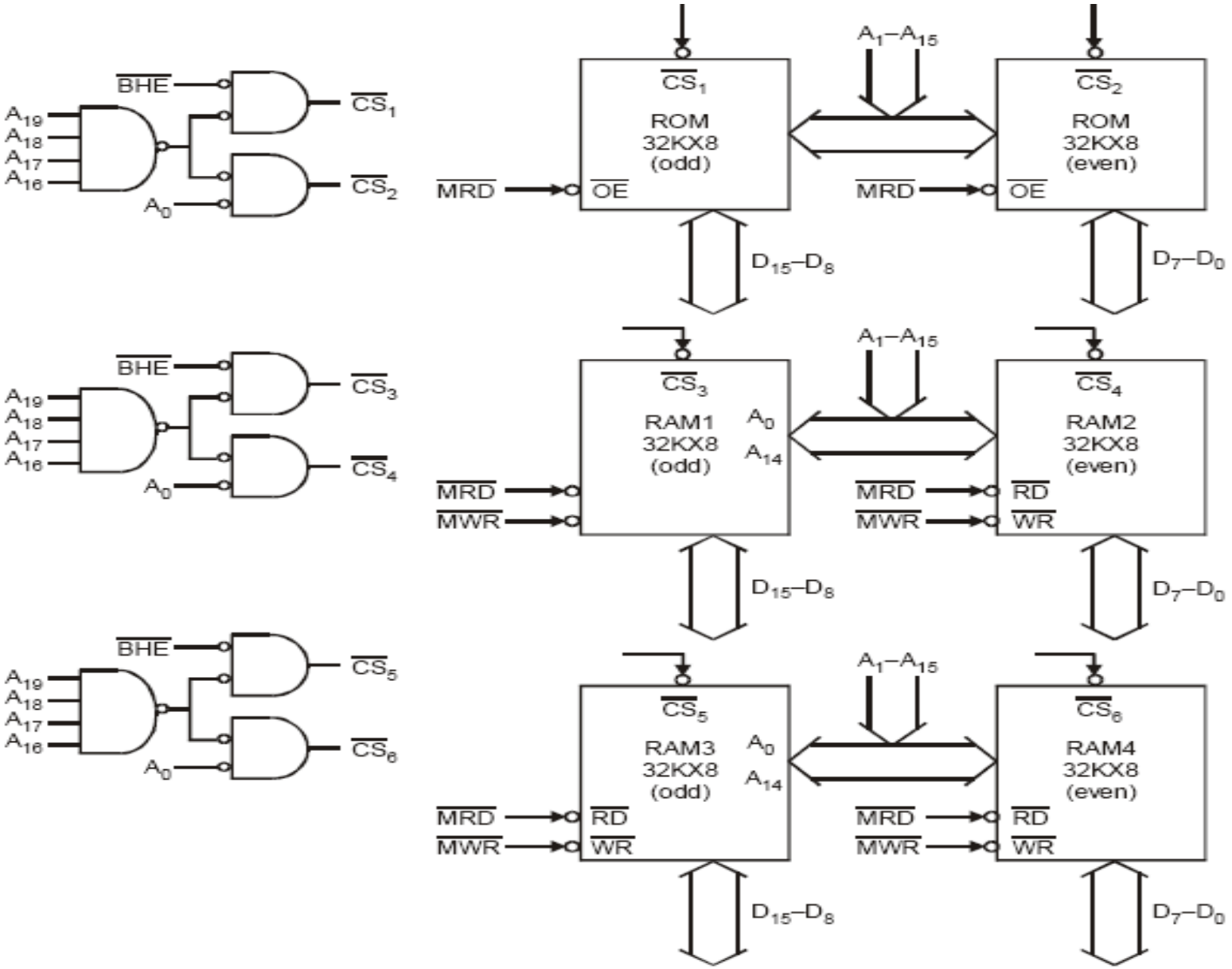


Fig. 5.53. Interfacing circuit.

- **DYNAMIC RAM INTERFA CING**
- When we require a large capacity of memory in a system, the memory subsystem is generally designed using D-RAM or dynamic RAM. D-RAM has variuos advantages of D-RAM such as :
- (1) Higher packaging density.
- (2) Lower cost.
- (3) Less power consumption

- Some disadvantages of D-RAM cell are as stated below :

(1) The D-RAM cell uses a capacitor to store the charge as a representation of data but the reverse biased diode has leakage current that tends to discharge the capacitor giving rise to the possibility of data loss.

(2) To avoid the data loss we must refresh the D-RAM cell after a fixed time interval.

(3) During the refreshing of the D-RAM all the operations of the memory are suspended hence resulting in

(a) Loss of time.

(b) Reduced system performance.

(4) The refresh mechanism and additional hardware required makesthe interfacing for D-RAM a complicated issue.

- A dedicated hardware chip called as D-RAM controller is the most important par t of the interfacing module. The (refresh cycle) is different from the memory read cycle in the following ways :

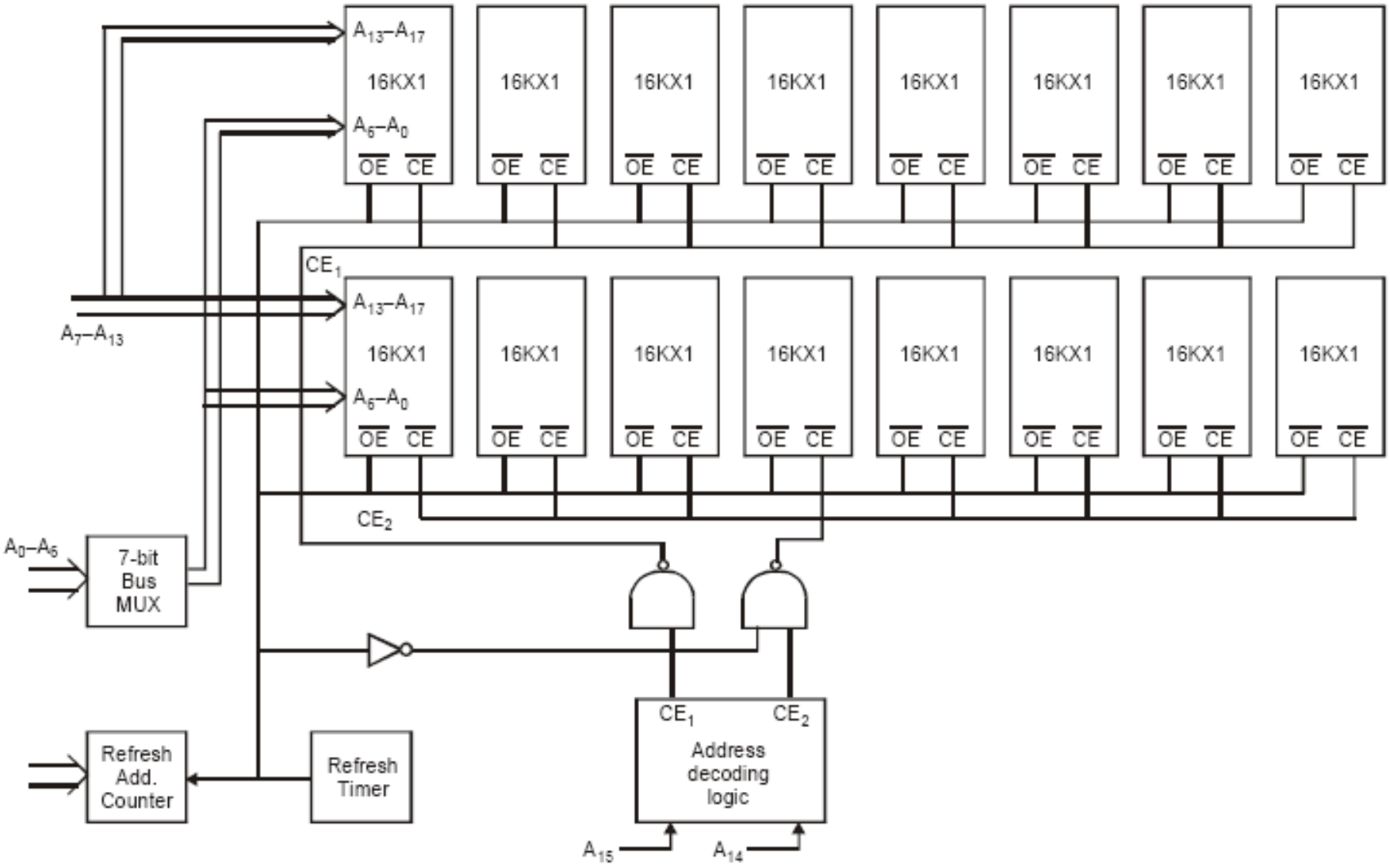
1. The memory address is not provided by the CPU address rather it is generated by a refresh mechanism counter called as refresh counter.
2. More than one memory chip may be enablled at a time so as to reduce the number of total memory refresh cycles.
3. Memory refresh is a independent regular activity initiated and carried out by the refresh mechanism whereas the memory read is either initiated by an external bus creator or a processor initiated operation.

- D-RAM is arranged internally in a 2-dimensional matrix away so that it will have n-rows and n-columns. A typical 4K bit D-RAM chip has an internally arranged bit array of dimensions 64 rows 64 columns. Thus the row address and the column address would require require 6 bits each. These 6 bits will be generated by the refresh counter during the refresh cycles. A complete row of 64 cells is refreshed at the same time to minimise the same time. Hence the refresh counter needs to generate only row addresses.

- The row addresses are than multiplexed over lower order address lines. The address bus of the processor is connected to the address bus of D-RAM during normal operations. A refresh timer devices a pulse for refreshing action after each refresh interval.
- **Refresh interval** is defined as the time for which a D-RAM cell can now data change level practically constant.
- **Procedence to calculate refresh interval :** The refresh interval depends upon the manufacturing technology of a D-RAm cell and may range between 1 ms–3 ms. Now let us consider 3 ms as the typical refresh time interval.

$$\text{Refresh time (per row)} \Rightarrow t_r = \frac{3 \times 10^{-3}}{64}$$

$$\text{Refresh frequency } f_r = \frac{64}{3 \times 10^{-3}} = 21.33 \times 10^3 \text{ Hz}$$


A13–A17
16KX1
A6–A0
OE
CE
CE1
A7–A13
CE2
A0–A6
7-bit
Bus
MUX
Refresh
Add.
Counter
Refresh
Timer
Address
decoding
logic
A15
A14

- The block diagram shows the refreshing logic and 8086 interfacing with D-RAM.
- Each of the chips used is a 16K 1 bit D-RA cell array. The system shown contains two 16K byte D-RAM units.
- The OE pin controls the output data buffers of the memory chips.
- The CE pins are active high chip selects of memory chips.

- **Refresh cycle :** If the refresh output of the refresh timer goes high, OE and CE also tend to go high.
- The high CE enables the memory chip for refreshing, while high OE prevents the data from appearing on the data bus. The 16K 1-bit D-RAM has an internal array of 128 128 cells requiring 7 bits for row addresses.
- The lower order seven lines A0-A6 are multiplexed with the refresh counter output A10-A16, as shown in the block diagram.

THANKS!

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