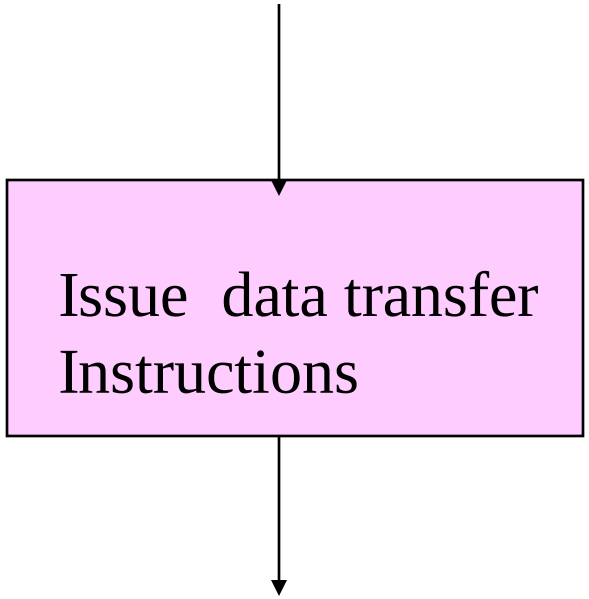
Microprocessor and Interfacing

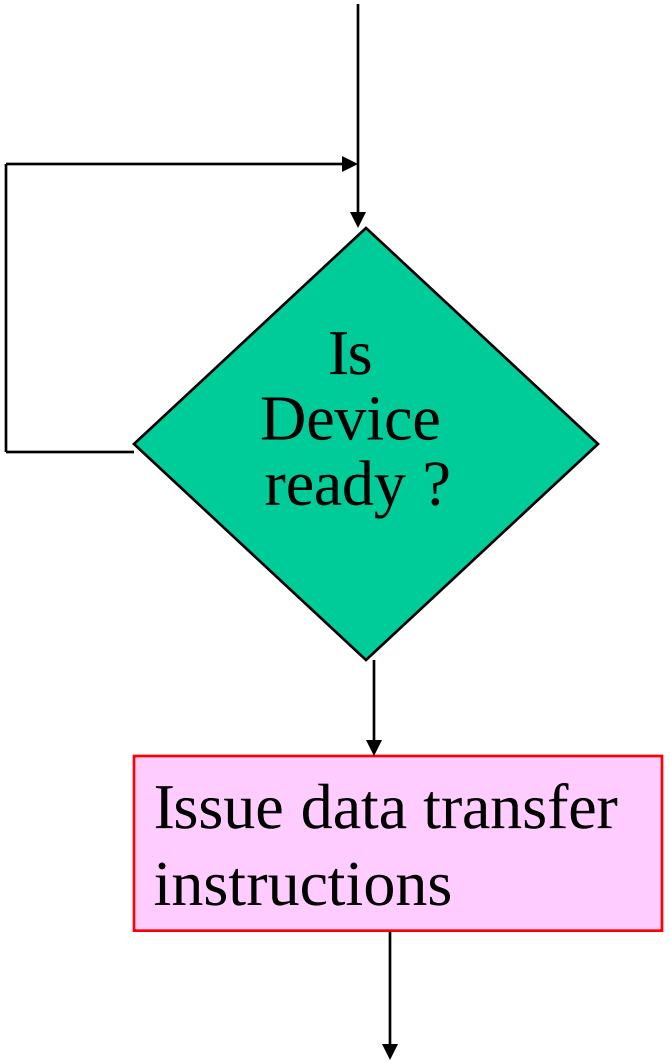
Interrupts

Data Transfer Schemes

- Programmed Data Transfer
  - Synchronous Data Transfer
  - Asynchronous Data Transfer
  - Interrupt Driven Data Transfer
- DMA



Synchronous Data Transfer

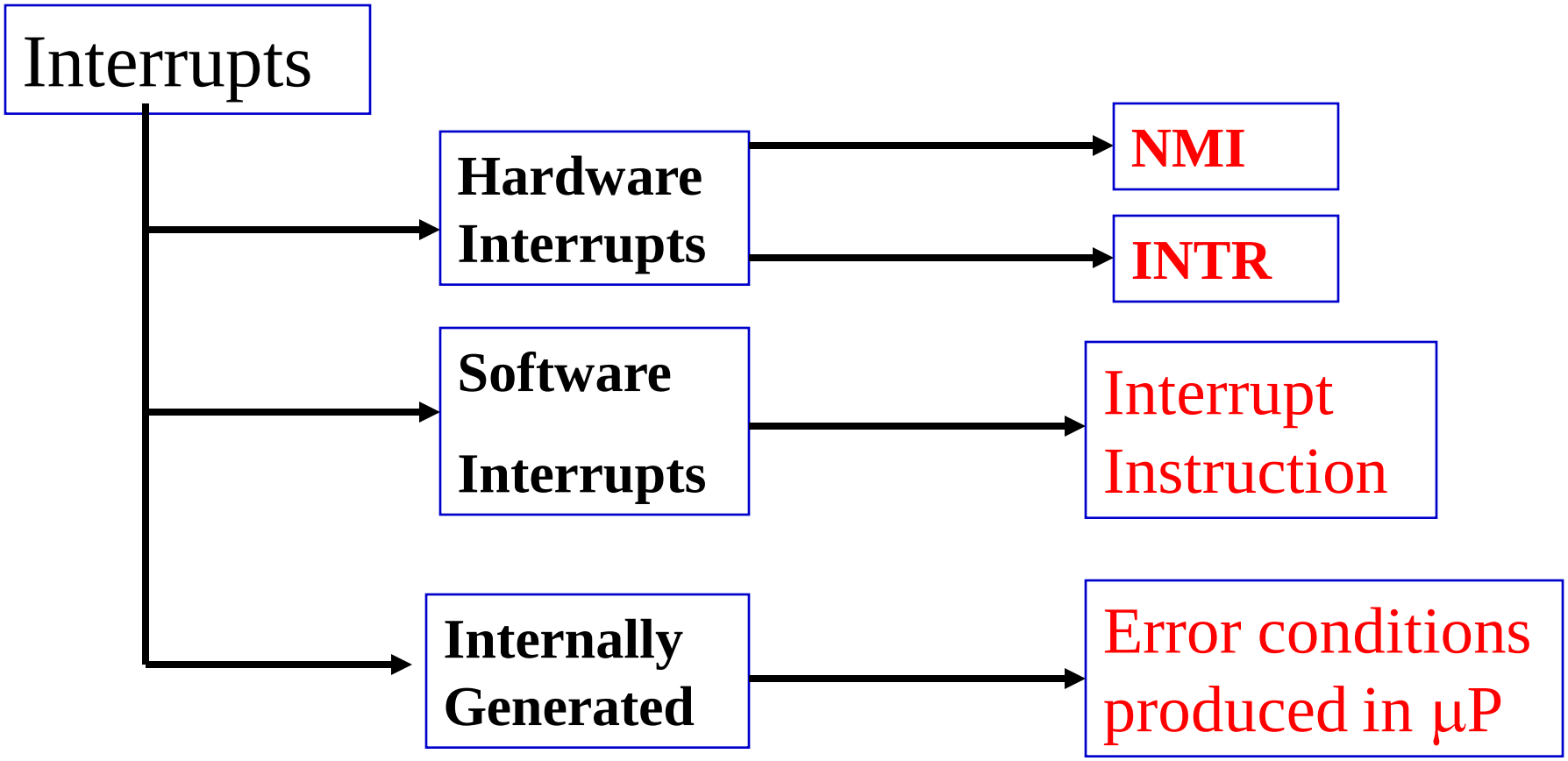


Asynchronous Data Transfer

Interrupt

An Interrupt is an input (internal or external) input to the microprocessor that causes microprocessor to suspend (interrupt) its normal operation and branch to a subroutine that services the interrupt.

Interrupt Classifications



x86 internals: **int, into, Divide Error, and Single Step**

“trap” generally means any processor generated interrupt;

in x86, usually means the Single Step interrupt

x86 Terminology for Interrupts:

1) Hardware Interrupt – External, uses INTR and NMI control bus lines

2) Software Interrupt – Internal, from **int** or **into**

3) Processor Interrupt – 2 Traps and 10 Software Interrupts (12 total)

Interrupt ***request*****:** a *signal* that immediate attention is needed

Interrupt ***processing*****:** what CPU does in response to request

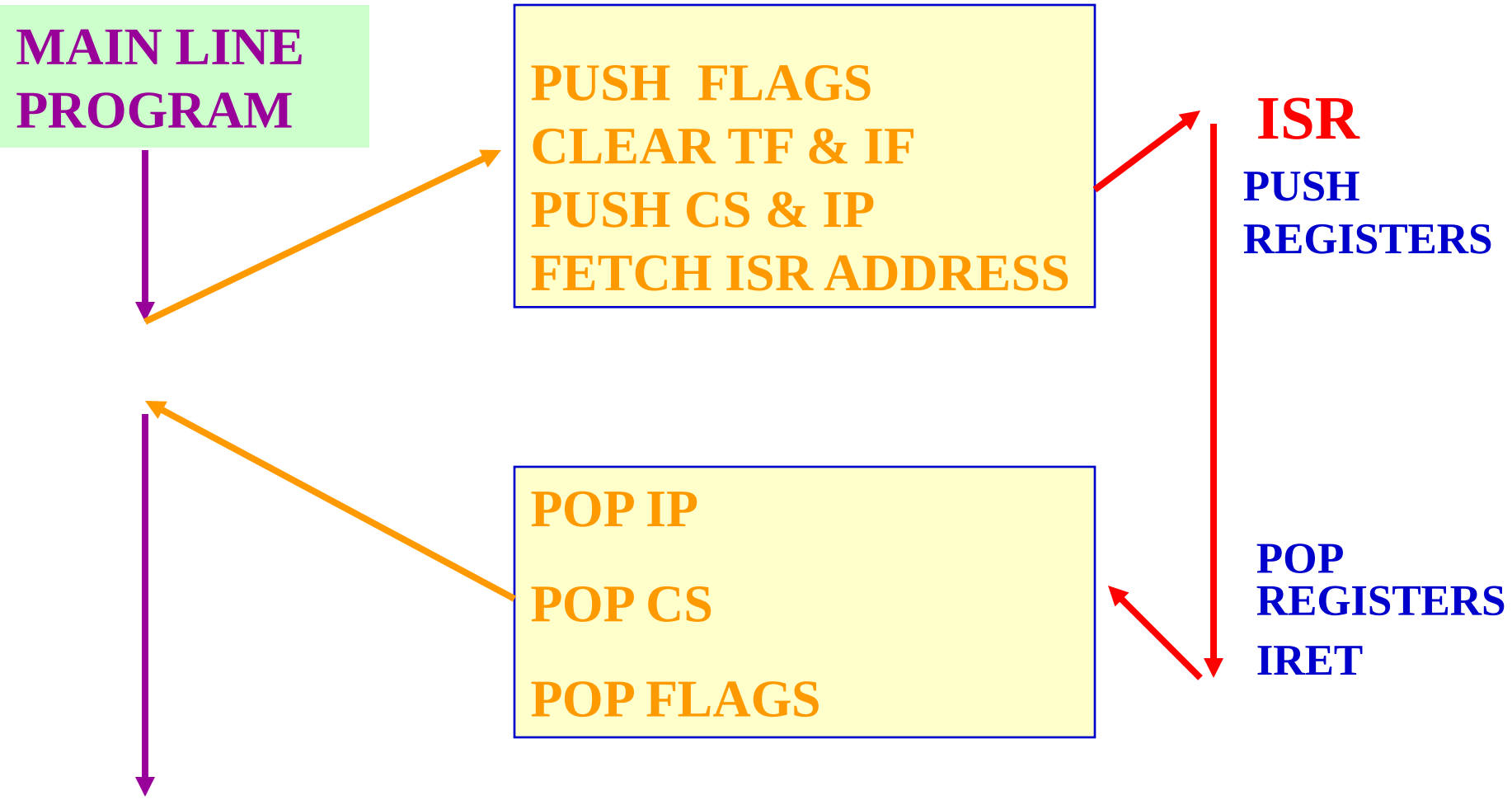
Interrupt ***service*****:** what is done in software as a result

2. General Types of Interrupts:

***External* -** generated outside CPU by other hardware

Internal - generated within CPU as a result of instruction or operation

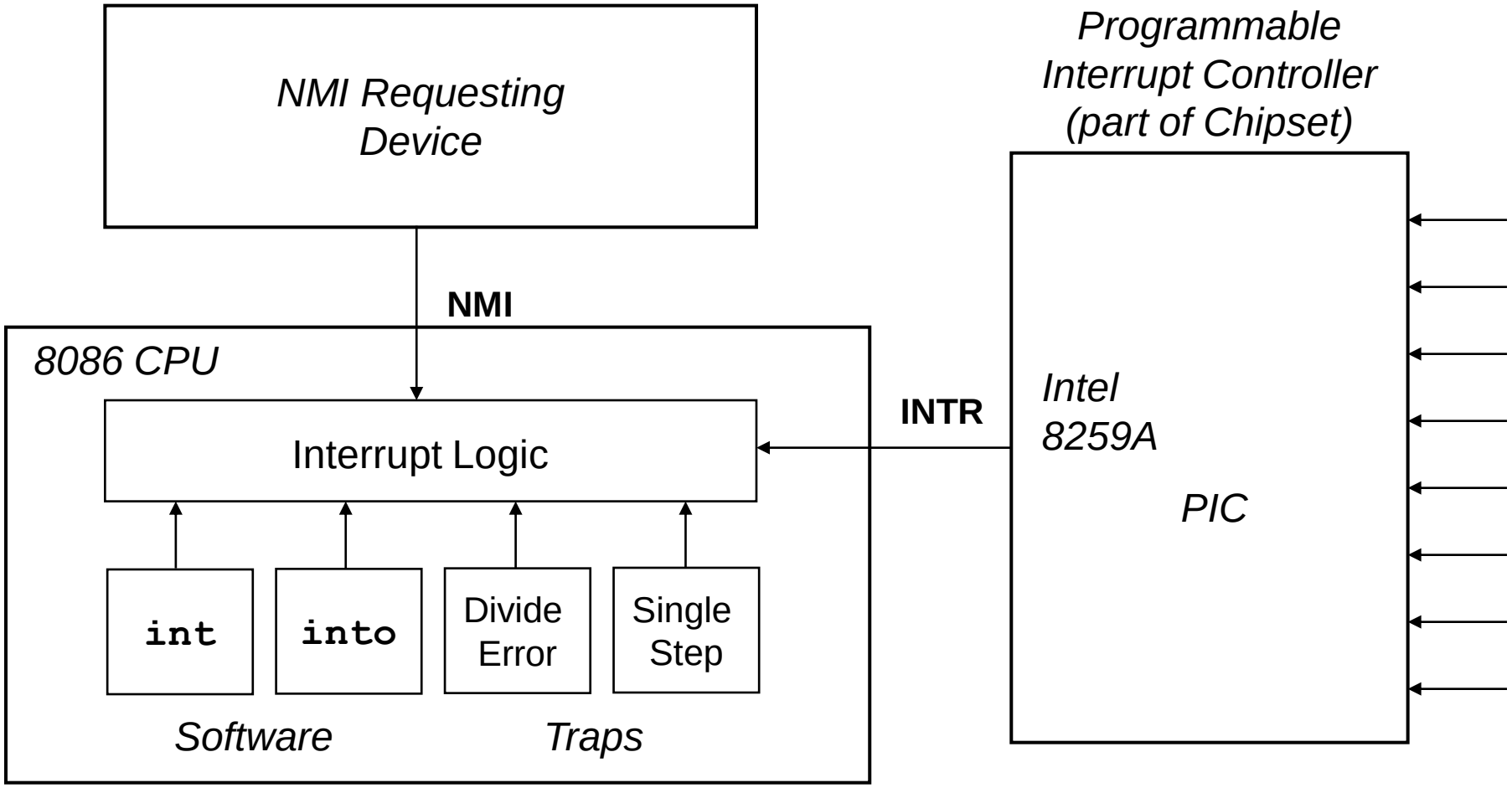
Interrupt Response



8086 External Interrupt Connections

NMI - *Non-Maskable Interrupt*

INTR - *Interrupt Request*



Interrupt Vector Table – IVT (in ***memory***)

- x86 has 256 Interrupts, specified by *Type Number* or *Vector*
- 1 Byte of data must accompany each interrupt; specifies *Type*
- *Vector* is a ***pointer*** (address) into *Interrupt Vector Table*, *IVT*
  - IVT is Stored in Memory from **`0000:0000`** to **`0000:03ffh`**
- *IVT* Contains 256 Far Pointer Values (Addresses)
  - Far Pointer is **`CS:IP`** Values
- Each Far Pointer is Address of *Interrupt Service Routine*, *ISR*
  - Also Referred to as *Interrupt Handler*
  - ***When interrupt is requested, which IVT entry? Type!***

8086 INTERRUPT TYPES

- Predefined Interrupts Type 0-4 (Total 5)
  - Divide by zero (Type 0)
  - Single Step (Type 1)
  - NMI (Pin) (Type 2)
  - Break Point (Type 3)
  - Interrupt on Over flow (Type 4)

* These 5 Interrupts are common to all µPs From 8086-Pentium 4

Single Step (Type-1) Interrupt

Setting up of Trap Flag (TP) automatically generates a type 1 interrupt

```
EXAMPLE:
PUSHF                ; SAVE FLAGS
MOV BP, SP           ;
OR   [BP+0]  WORD PTR  0100H    ; SET  TF
AND  [BP+0]  WORD PTR  FEFFH    ; CLEAR TP
POPF
```

SETTING UP TF :EXAMPLE 12.1

```
TRON PROC NEAR
        PUSH   AX
        PUSH   BP
        MOV  BP, SP
        MOV  AX, [BP+8]     ; GET FLAGS FROM STACK.
        OR      AH, 01           ; SET UP TRAP FLAG
        AND    AH, 0FEH       ; CLEAR TRAP FLAG
        MOV  [BP + 8] ; AX
        POP   BP
        POP   AX
        IRET
TRON ENDP
```

Software Interrupts

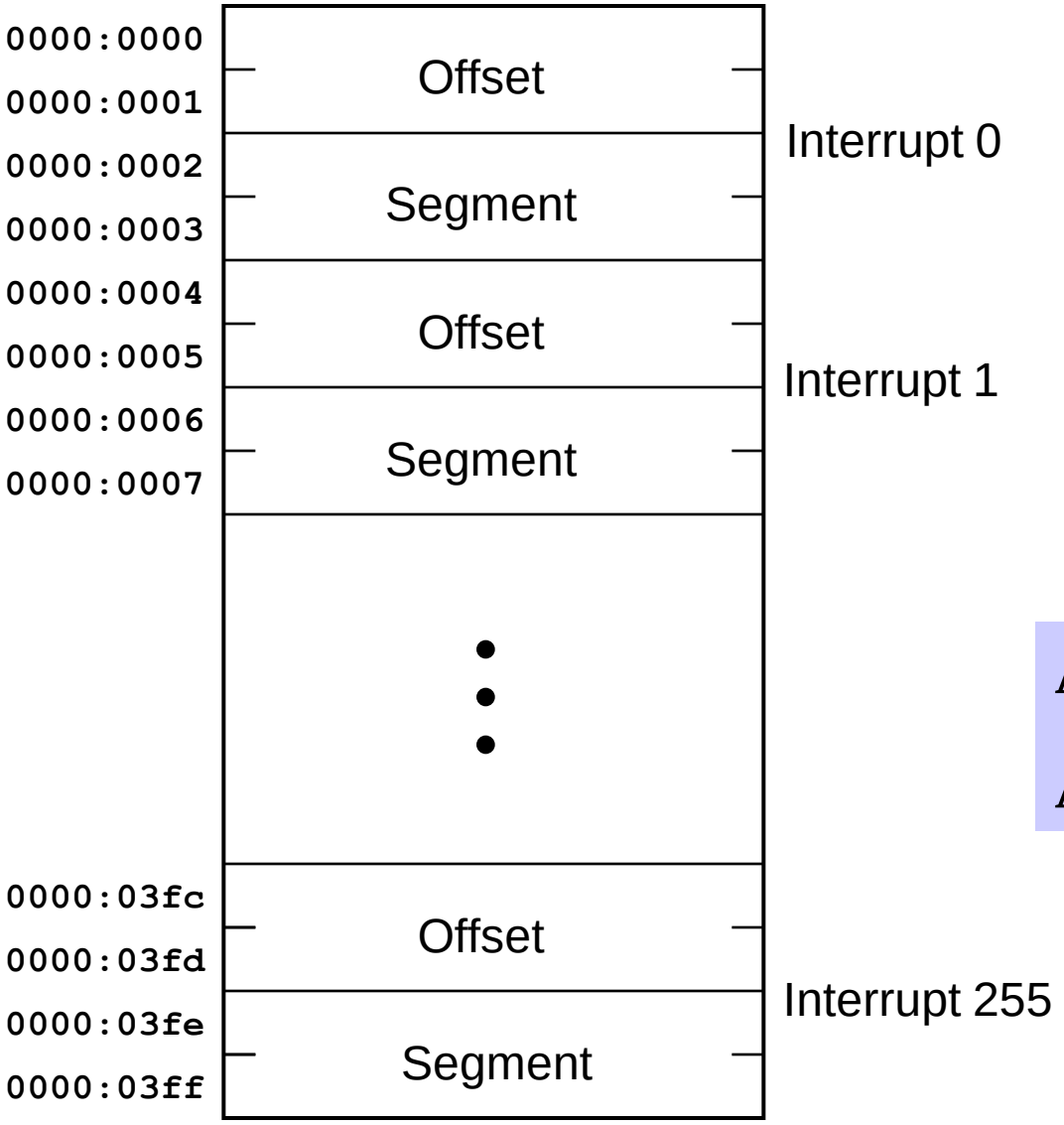
- These interrupts can be generated using an **INT nn** instruction.
- Type code 0 - 255 can be used with INT nn instruction
- USES
  - These allow us to test ISR for Hardware Interrupts without the actual hardware interrupts

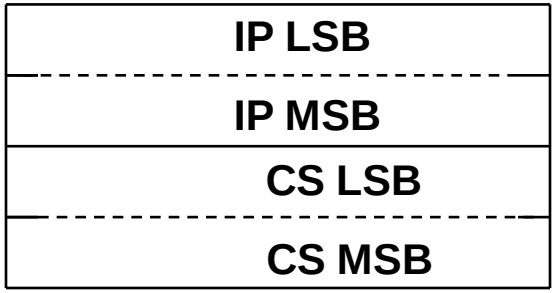
Type 0:	Divide by 0 error
Type 1	Single Step
Type 2	NMI
Type 3	One byte Break Point
Type 4	Overflow INTO

INTR- Interrupts
(User Defined Type 32 to 255)

- Maskable with the help of IF (0 = disabled)
- Masking can be done with CLI instruction
- INTR can be enabled with STI instruction
- INTR is LEVEL activated.
- On RESET IF is cleared (ALL flags cleared). Why?
- On INTR, IF is automatically cleared. Why?

IVT Format





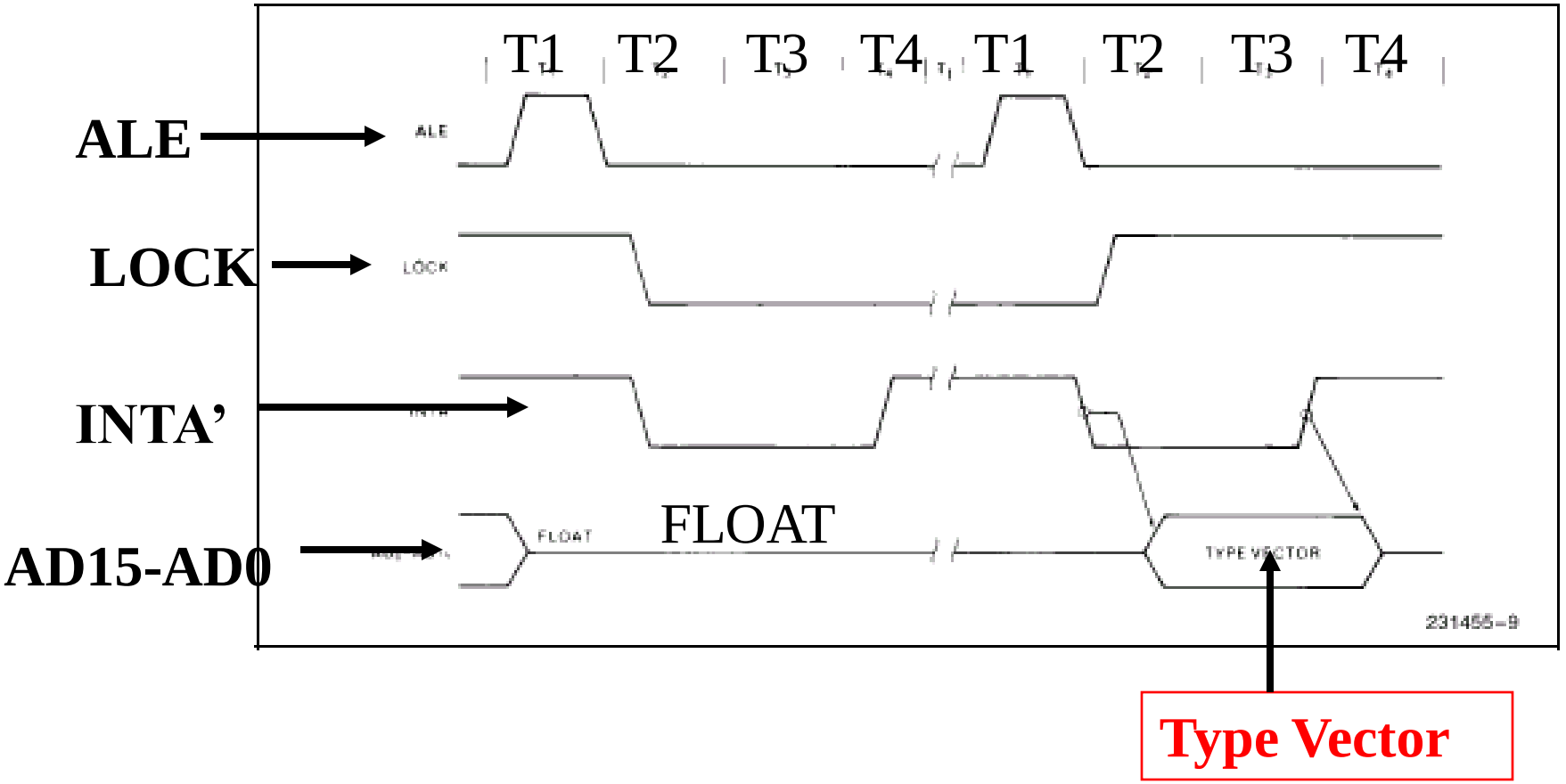
Given a Vector, where is the ISR address stored in memory ?

Add. for IP = TYPE *4

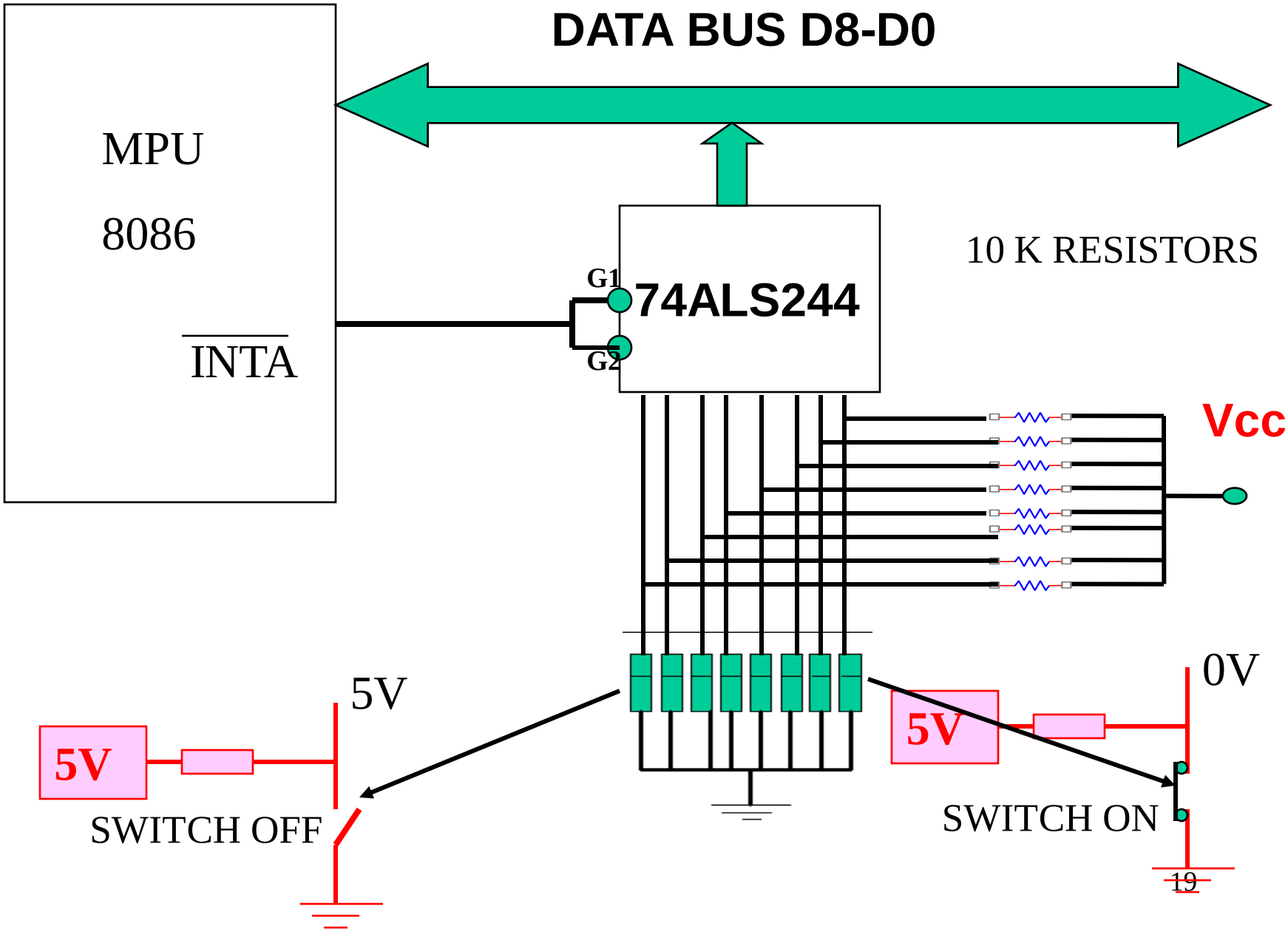
Add for CS = TYPE* 4 + 2

Example: **`int 36h`**
Offset = (54×4) = 216
= **`00d8h`**

Interrupt Acknowledge Machine Cycle



GENERATING AN IVT



`Halt` Instruction

- This instruction causes processor to enter a HALT state
- HALT state is one where no further instructions are fetched or executed until one of the following events occurs:

  1) System is Reset - Rising Edge on RESET pin

  2) External Interrupt Occurs

CPU Asset	Content
FLAGS Register	**0000h**
IP	**0000h**
CS	**ffffh**
DS	**0000h**
SS	**0000h**
ES	**0000h**
Instruction Queue	Empty

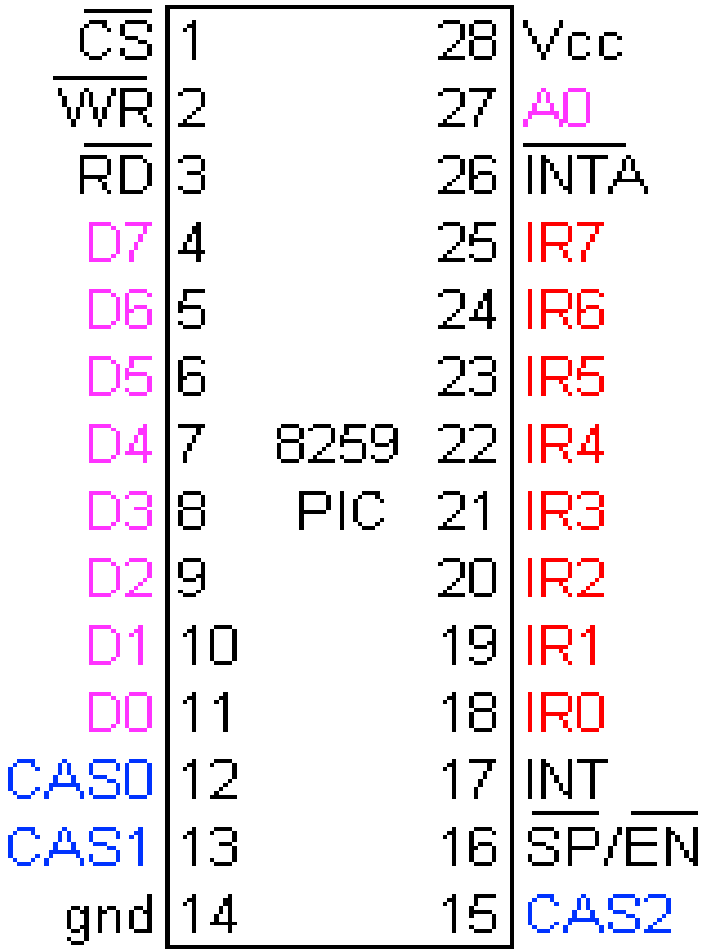
Interrupt Vector Assignments

Type	Function	Comment
0	Divide Error	Processor - zero or overflow
1	Single Step (DEBUG)	Processor - TF=1
2	Nonmaskable Interrupt Pin	Processor - NMI Signal
3	Breakpoint	Processor - Similar to Sing Step
4	Arithmetic Overflow	Processor - into
5	Print Screen Key	BIOS - Key Depressed
6	Invalid Opcode	Processor - Invalid Opcode
7	Coprocessor Not Present	Processor - no FPU
8	Time Signal	BIOS - From RT Chip (AT - IRQ0)
9	Keyboard Service	BIOS - Gen Service (AT - IRQ1)
A - F	Originally Bus Ops (IBM PC)	BIOS - (AT - IRQ2-7)
10	Video Service Request	BIOS - Accesses Video Driver
11	Equipment Check	BIOS - Diagnostic
12	Memory Size	BIOS - DOS Memory
13	Disk Service Request	BIOS - Accesses Disk Driver
14	Serial Port Service Request	BIOS - Accesses Serial Port Drvr
15	Miscellaneous	BIOS - Cassette, etc.
16	Keyboard Service Request	BIOS - Accesses KB Driver

Interrupt Vector Assignments (cont)

Type	Function	Comment
17	Parallel Port LPT Service	BIOS - Printer Driver
18	ROM BASIC	BIOS - BASIC Interpreter in ROM
19	Reboot	BIOS - Bootstrap
1A	Clock Service	BIOS - Time of Day from BIOS
1B	Control-Break Handler	BIOS - Keyboard Break
1C	User Timer Service	BIOS - Timer Tick
1D	Pointer to Video Parm Table	BIOS - Video Initialization
1E	Pointer to Disk Parm Table	BIOS - Disk Subsystem Init.
1F	Pointer to Graphics Fonts	BIOS - CGA Graphics Fonts
20	Program Terminate	DOS - Clear Memory, etc.
21	Function Call	DOS - Transfer Control
22	Terminate Address	DOS - program Terminate handler
23	Control-C Handler	DOS - For OS Use
24	Fatal Error Handler	DOS - Critical Error
25	Absolute Disk Read	DOS - Disk Read
26	Absolute Disk Write	DOS - Disk Write
27	Terminate	DOS - TSR Usage
28	Idle Signal	DOS - Idle
2F	Print Spool	DOS - Cassette, etc.
70-77	Hardware Interrupts in AT Bios	DOS - (AT - IRQs 8-15)

Intel 8259


CS 1
WR 2
RD 3
D7 4
D6 5
D5 6
D4 7
D3 8
D2 9
D1 10
D0 11
CAS0 12
CAS1 13
gnd 14
8259
PIC
28 Vcc
27 A0
26 INTA
25 IR7
24 IR6
23 IR5
22 IR4
21 IR3
20 IR2
19 IR1
18 IR0
17 INT
16 SP/EN
15 CAS2

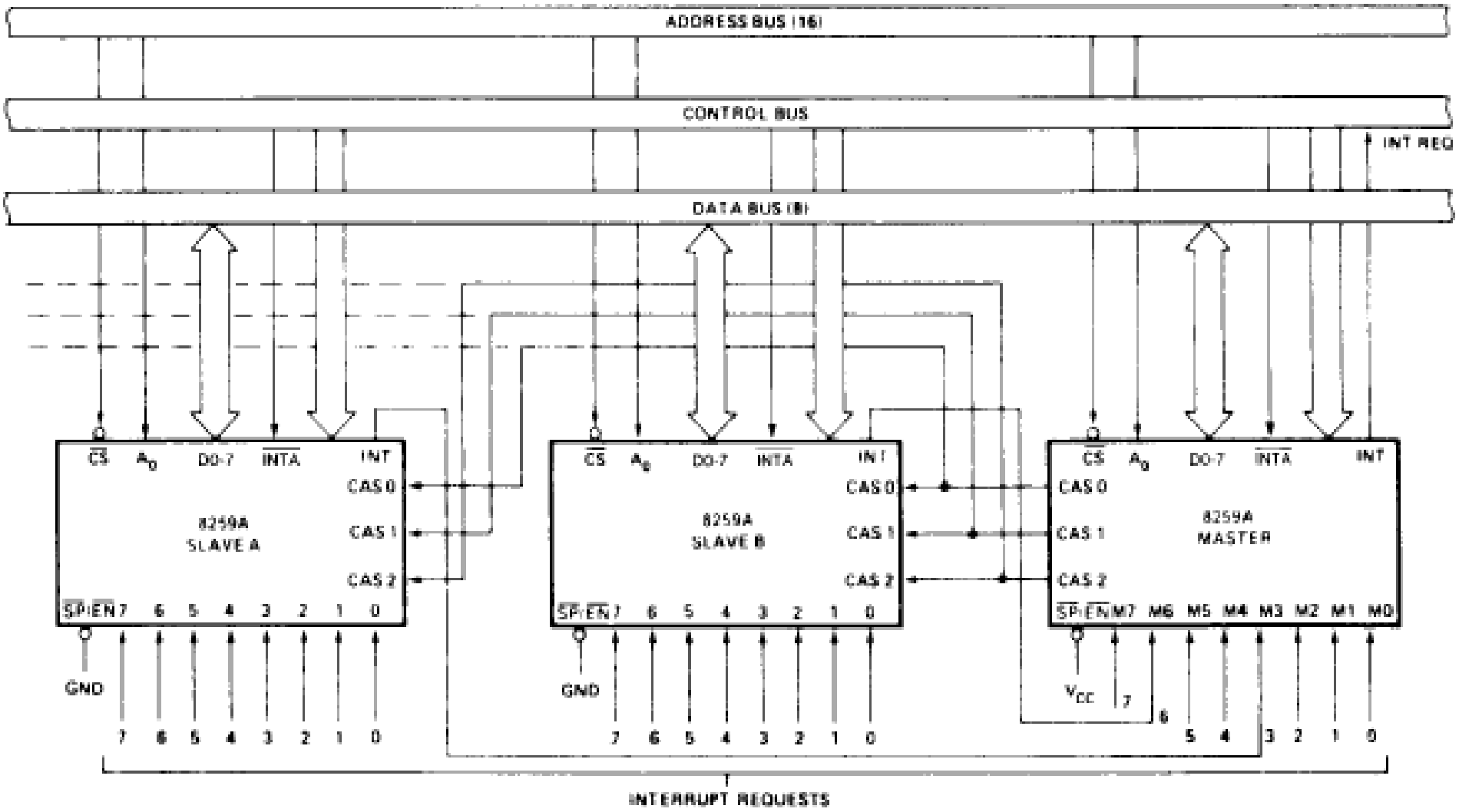
Features

- 8086, 8088 Compatible
- MCS-80, MCS-85 Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single 5V Supply (No Clocks)
- Available in 28-Pin DIP and 28-Lead PLCC Package

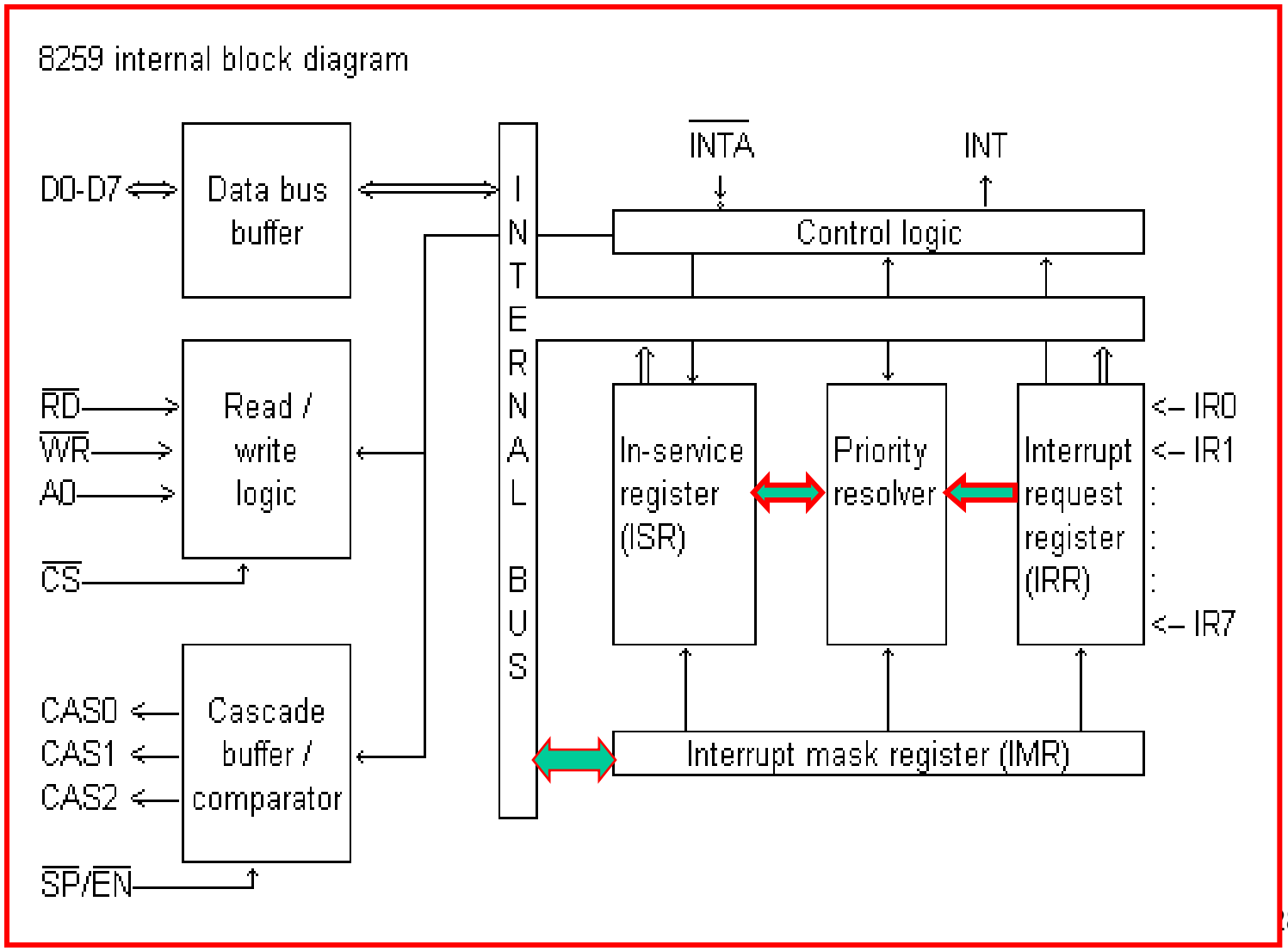
PIN Functions

- D0-D7: Bi-directional, tristated, buffered data lines. Connected to data bus directly or through buffers
- RD-bar: Active low read control
- WR-bar: Active low write control
- A0: Address input line, used to select control register
- CS-bar: Active low chip select
- IR0-7: Asynchronous IRQ input lines, generated by peripherals.

- CAS0-2: Bi-directional, 3 bit cascade lines. In master mode, PIC places slave ID no. on these lines. In slave mode, the PIC reads slave ID no. from master on these lines. It may be regarded as slave-select.
- SP-bar / EN-bar: Slave program / enable. In non-buffered mode, it is SP-bar input, used to distinguish master/slave PIC. In buffered mode, it is output line used to enable buffers.
- INT: Interrupt line, connected to INTR of microprocessor
- INTA-bar: Interrupt ack, received active low from microprocessor


ADDRESS BUS (16)
CONTROL BUS
INT REQ
DATA BUS (8)
CS
A0
D0-7
INTA
INT
CAS 0
CAS 1
CAS 2
8259A
SLAVE A
SP/EN
7 6 5 4 3 2 1 0
GND
8259A
SLAVE B
8259A
MASTER
M7 M6 M5 M4 M3 M2 M1 M0
VCC
INTERRUPT REQUESTS

BLOCK DIAGRAM OF 8259



Interrupt Sequence (Single PIC & 8085 based systems)

- One or more of the IR lines goes high. Corresponding IRR bit is set.
- 8259 evaluates the request and sends INT to CPU.
- CPU sends INTA-bar.
- Highest priority ISR is set. IRR is reset. 8259 releases CALL instruction on data bus.
- CALL causes CPU to initiate two more INTA-bar's.
- 8259 releases the subroutine address, first low byte then high byte.
- ISR bit is reset depending on mode. In the AEOI mode the ISR bit is set at the end of third INTA-bar pulse. Otherwise EOI bit remains set until appropriate command is issued at the end of interrupt sequence.

Interrupt Sequence (Single PIC & 8086 μP based systems)

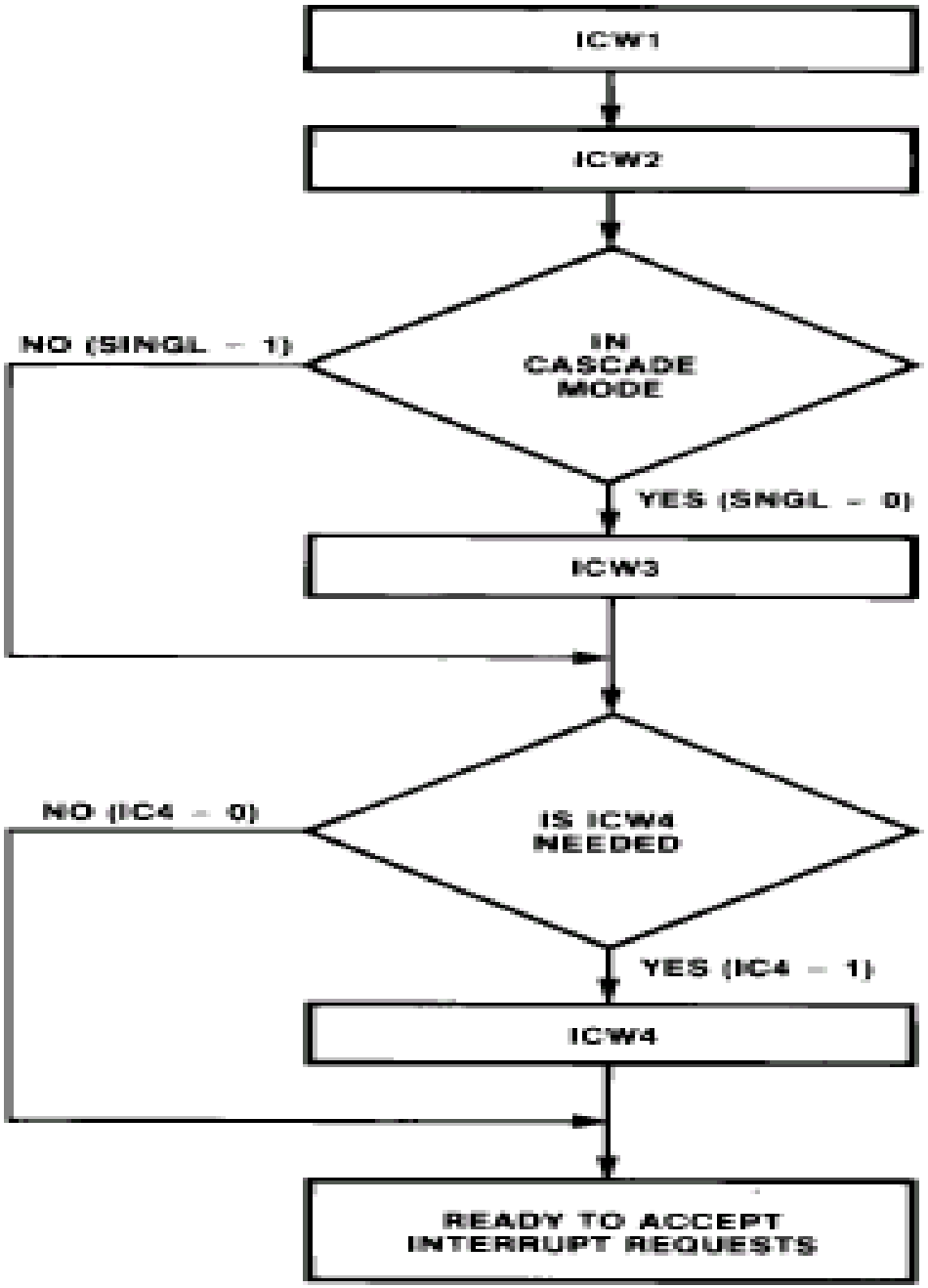
1. One or more of the IR lines goes high. Corresponding IRR bit is set.
2. 8259 evaluates the request and sends INT to CPU.
3. CPU sends INTA-bar.
4. Highest priority ISR is set. IRR is reset. 8259 does not drive data bus during this cycle.
5. In the second m/c when INTA-bar signal is asserted, 8259 releases the 8 bit type vector on the data bus that is read by the CPU.
6. ISR bit is reset depending on mode. In the AEOI mode the ISR bit is set at the end of second INTA-bar pulse. Otherwise EOI bit remains set until appropriate command is issued at the end of interrupt subroutine.

PROGRAMMING 8259

The 8259A accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs): Before normal operation can begin, each 8259A in the system must be brought to a starting point–by a sequence of 2 to 4 bytes timed by WR pulses.
2. Operation Command Words (OCWs): These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
    a. Fully nested mode
    b. Rotating priority mode
    c. Special mask mode
    d. Polled mode

   The OCWs can be written into the 8259A anytime after initialization.


ICW1
ICW2
IN CASCADE MODE
NO (SINGL = 1)
YES (SNGL = 0)
ICW3
IS ICW4 NEEDED
NO (IC4 = 0)
YES (IC4 = 1)
ICW4
READY TO ACCEPT INTERRUPT REQUESTS

Whenever a command is issued with A0 = 0 and D4 =1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the intiitalization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transistion to generate an interrupt.

b. The Interrupt Mask Register is cleared.

c. IR7 input is assigned priority 7.

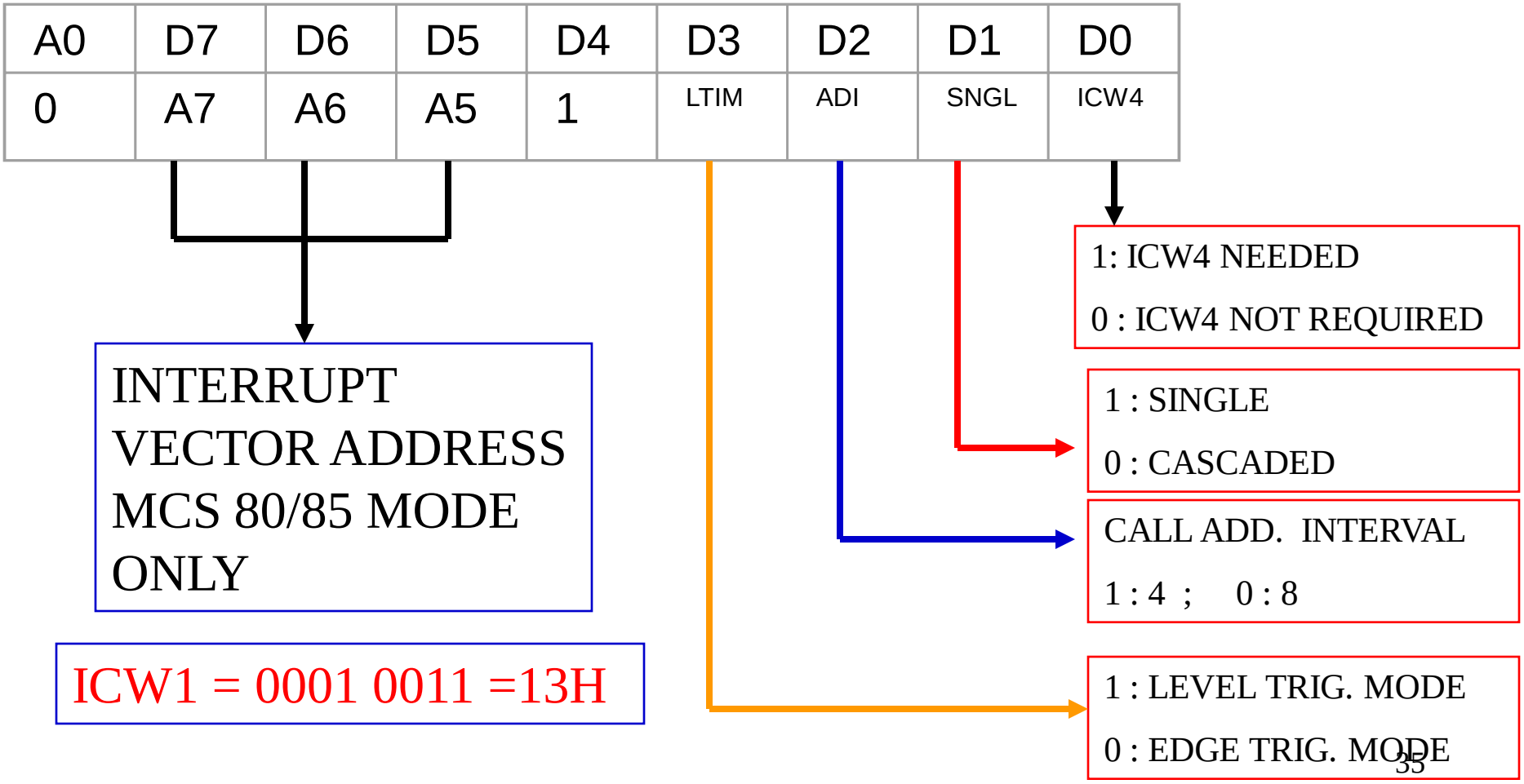
d. The slave mode address is set to 7.

e. Special Mask Mode is cleared and Status Read is set to IRR.

f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto EOI, MCS-80, 85 system).

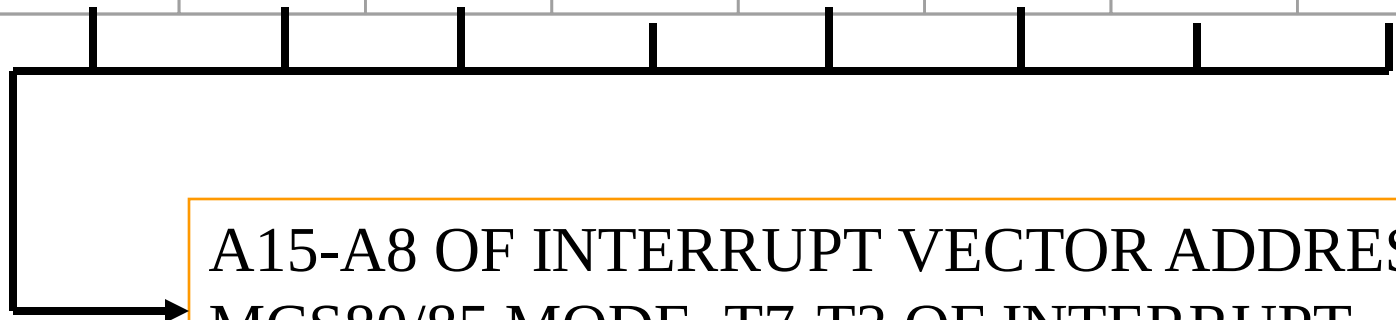
*NOTE: Master/Slave in ICW4 is only used in the buffered mode.

ICW-1


A0 D7 D6 D5 D4 D3 D2 D1 D0
0 A7 A6 A5 1 LTIM ADI SNGL ICW4
1: ICW4 NEEDED
0 : ICW4 NOT REQUIRED
INTERRUPT VECTOR ADDRESS MCS 80/85 MODE ONLY
1 : SINGLE
0 : CASCADED
CALL ADD. INTERVAL
1 : 4 ; 0 : 8
ICW1 = 0001 0011 =13H
1 : LEVEL TRIG. MODE
0 : EDGE TRIG. MODE

ICW-2

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	A15/T7	A14/T6	A13/T5	A12/T4	A11/T3	A10	A9	A8



A15-A8 OF INTERRUPT VECTOR ADDRESS MCS80/85 MODE. T7-T3 OF INTERRUPT VECTOR ADDRESS 8086/8088 MODE

TYPES 0 TO 31 ARE RESERVED.

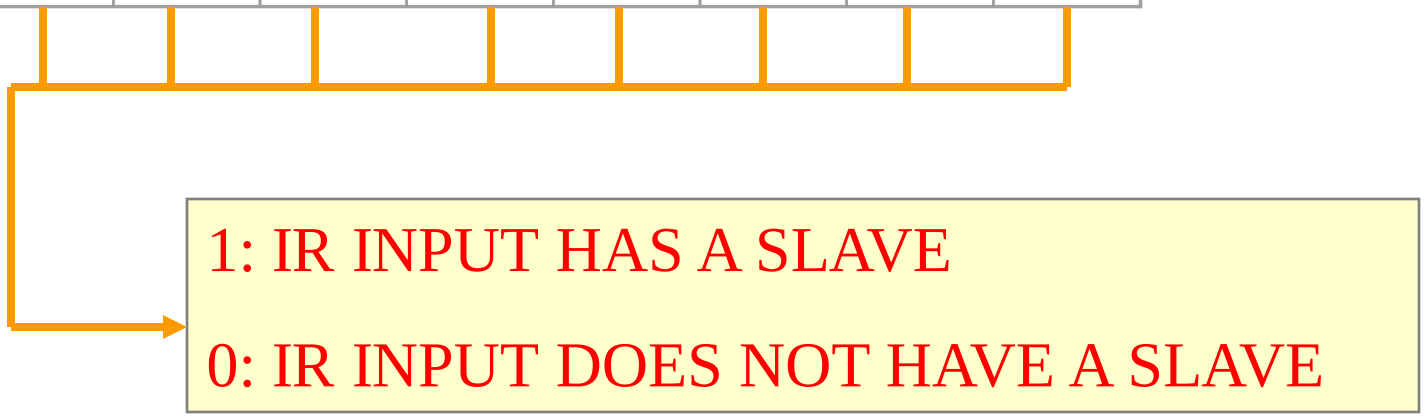
ICW 2 = 0010 0000 = 20H = TYPE 32 INTERRUPT

CONTENTS OF INTERRUPT VECTOR BYTE

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

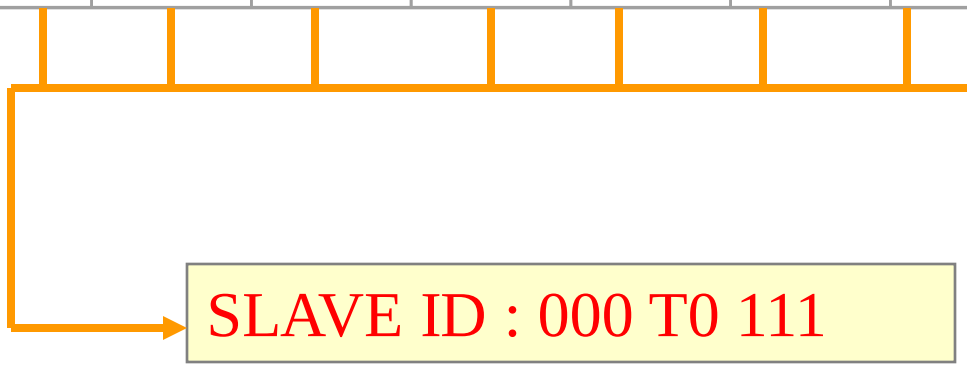
ICW-3 (MASTER DEVICE)

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	S7	S6	S5	S4	S3	S2	S1	S0



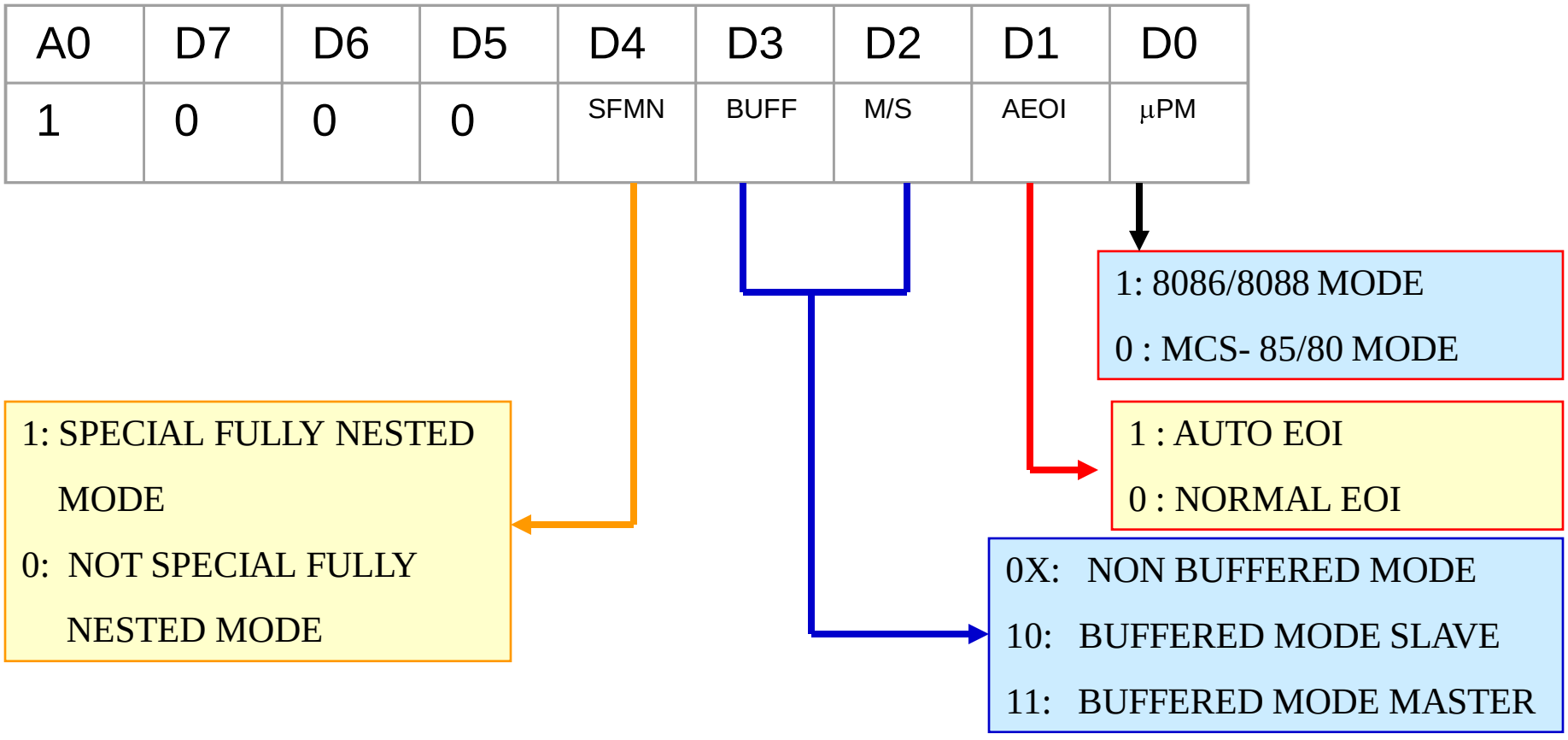
ICW3 (SLAVE DEVICE)

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	ID2	ID1	ID0



ICW- 4

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SFMN	BUFF	M/S	AEOI	μPM



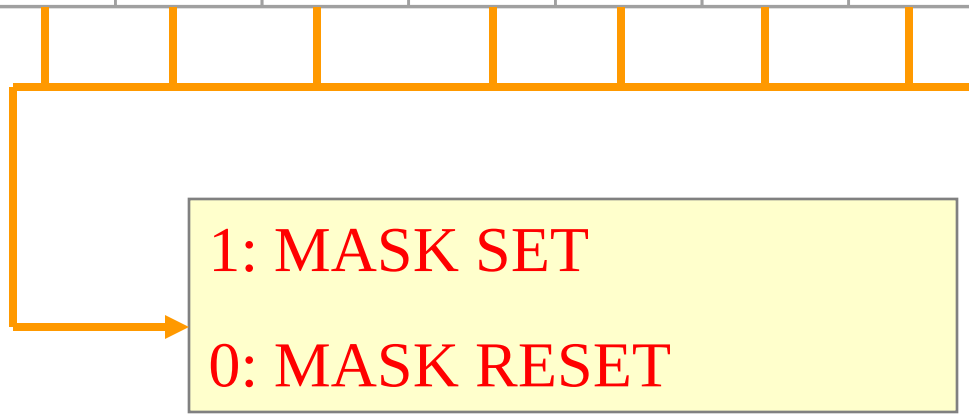
OPERATIONAL CONTROL WORD

- These are the command words which command the 8259 in various interrupt modes.
  - FULLY NESTED
  - ROTATING PRIORITY
  - SPECIAL MASK MODE
  - POLLED MODE

  OCWs can be written any time after initialization of 8259.

OCW-1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0



OCW-2

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	R	SL	EOI	0	0	L2	L1	L0

001: NON SPECIFIC EOI COMMAND

011: SPECIFIC EOI COMMAND

101: ROTATE ON NON SPECIFIC EOI

100: ROTATE IN AUTOMATIC EOI MODE (SET)

000: ROTATE IN AUTOMATIC EOI MODE (CLEAR)

111: ROTATE ON SPECIFIC EOI COMMAND

110: SET PRIORITY COMMAND

010: NO OPERATION

000 TO 111: INTERRUPT LEVEL TO BE ACTED UPON (0 TO 7)

OCW-3

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	ESMM	SMM	0	1	P	RR	RIS

00: NO ACTION

01: NO ACTION

10: RESET SPECIAL MASK MODE

11: SET SPECIAL MASK MODE

1: POLE COMMAND

0: NO POLL COMMAND

00: NO ACTION

01: NO ACTION

10: READ IRR ON NEXT READ PULSE

11: READ ISR ON NEXT READ PULSE

Fully Nested Mode (Cont.)

- After the initialization sequence, IR0 has the highest prioirity and IR7 the lowest.
- Priorities can be changed, as will be explained, in the rotating priority mode.

Queries

Any questions related to the topic can be mailed to me at

nikhilmarriwala@hotmail.com

Or can sought out here only in the class.
Queries

THANKS!

For more Notes Follow http://www.edutechlearners.com