Intel 8086 Pin Functions

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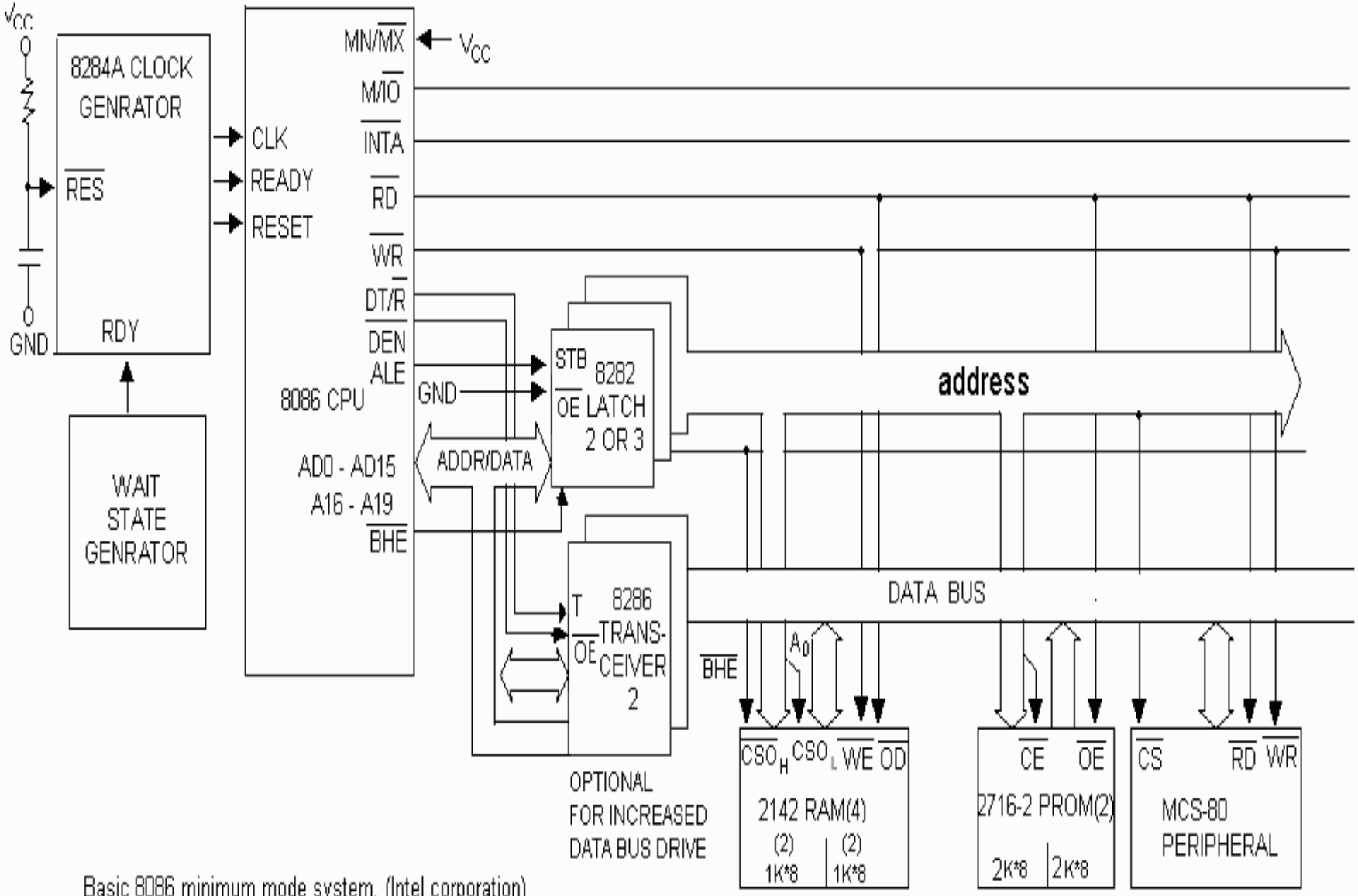
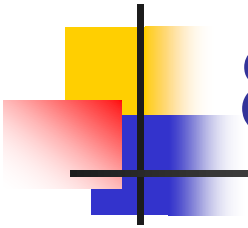
80x86 Processor Overview

Product	***8008***	***8080***	***8085***	***8086***	***8088***	***80286***	***80386***	***80486***	***Pent.***	***Pent. Pro***
Year Introduced	1972	1974	1976	1978	1979	1982	1985	1989	1992	1995
Technology	PMOS	NMOS	NMOS	NMOS	NMOS	NMOS	CMOS	CMOS	BICMOS	BICMOS
Clock Rate	0.5-0.8	2-3	3-8	5-10	5-8	10-16?	16-40	66	60-66+	150
Number of Pins	18	40	40	40	40		132	168	273	387
Number of transistors	3000	4500	6500	29K	29K	130K	275K	1.2M	3M	5.5M
Number of instructions	66	111	113	133	133					
Physical Memory	16K	64K	64K	1M	1M	16M	16M4GB	4GB	4GB	64G
Virtual Memory	none	none	none	none	none	1G	64T	64T	64T	64T
Internal Data Bus	8	8	8	16	16	16	32	32	64	32
External Data Bus	8	8	8	16	8	16	16,32	32	64	64
Address Bus	8	16	16	20	20	24	24,32	32	32	36
Data Types	8	8	8	8,16	8,16	8,16	8,16,32	8,16,32	8,16,32	8,16,32

MIN MODE SYSTEM



Basic 8086 minimum mode system. (Intel corporation)



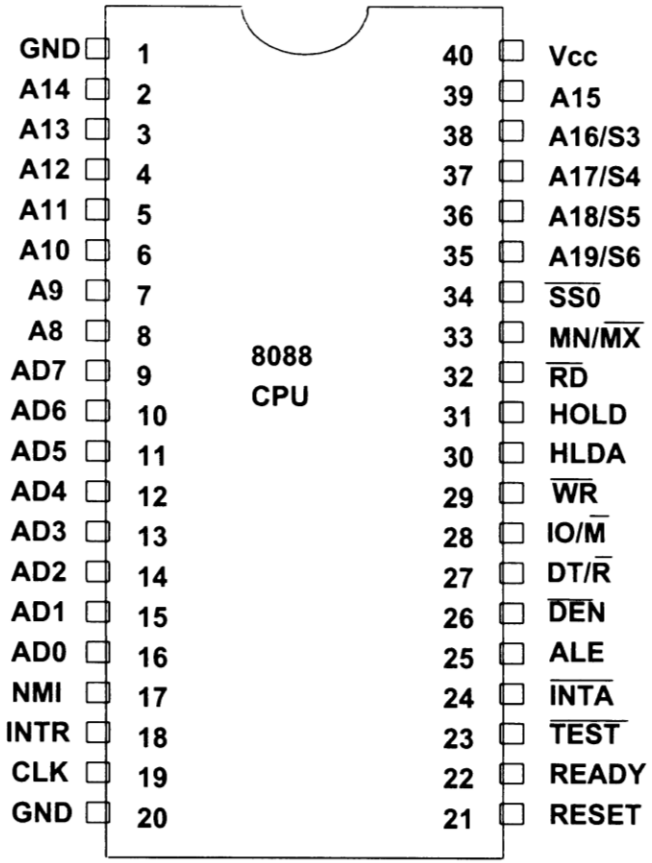
8088/8086 Microprocessor

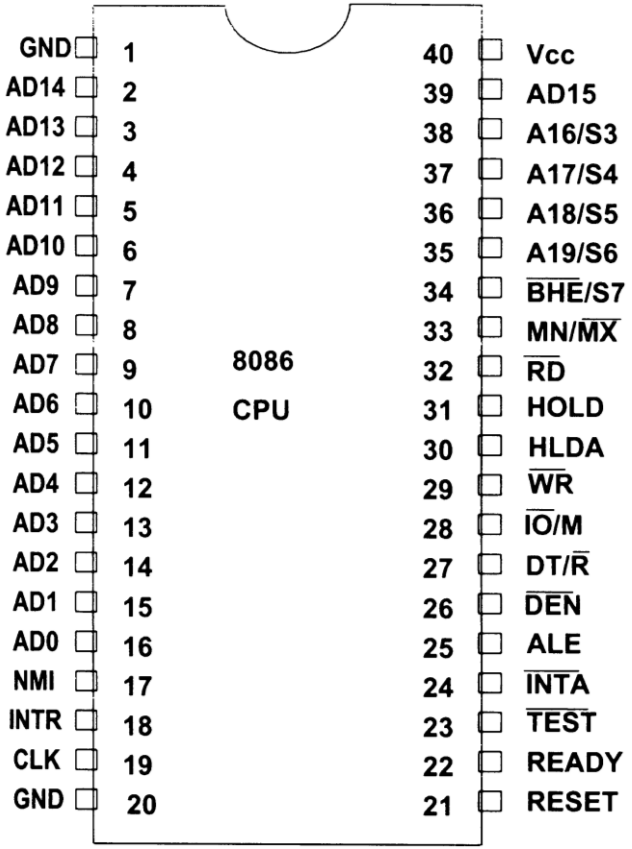
- Both 40 pin packages
- Data bus
  - Both 16 bit internally
  - 8088 is 8 bit externally – use AD0-AD7
  - 8086 is 16 bit externally – use AD0-AD15
  - ALE (Address Latch Enable) Low indicates the data is actually data, not an address
- Data but and address bus multiplexed to same pins!

8088/8086 Microprocessor

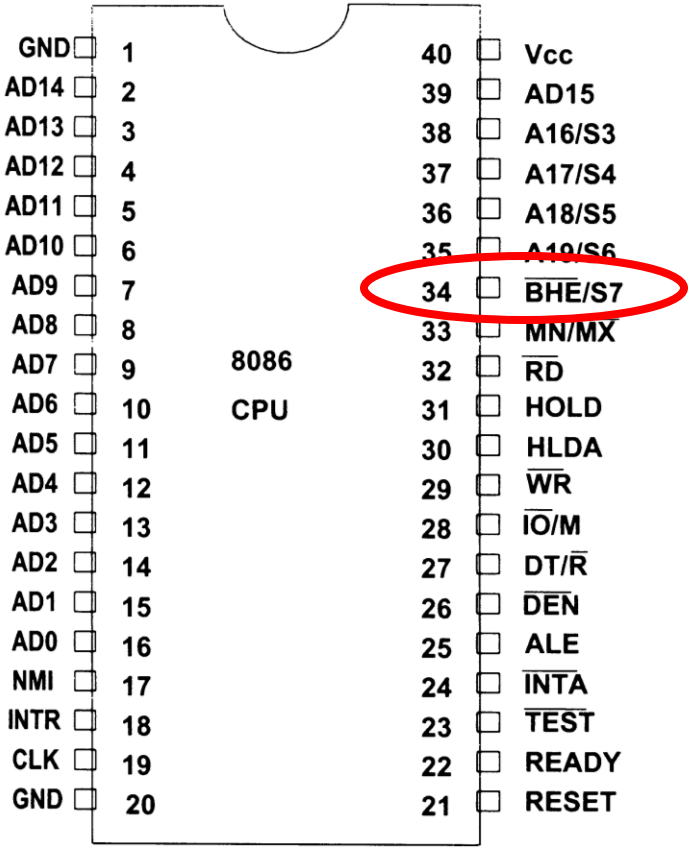
- Address bus
  - ALE must be set high
  - Most common latch: 74LS373
    - Receives AD0-AD7 (8088) or AD0-AD15 (8086) and ALE

8088/8086 Pin Out (Min Mode)



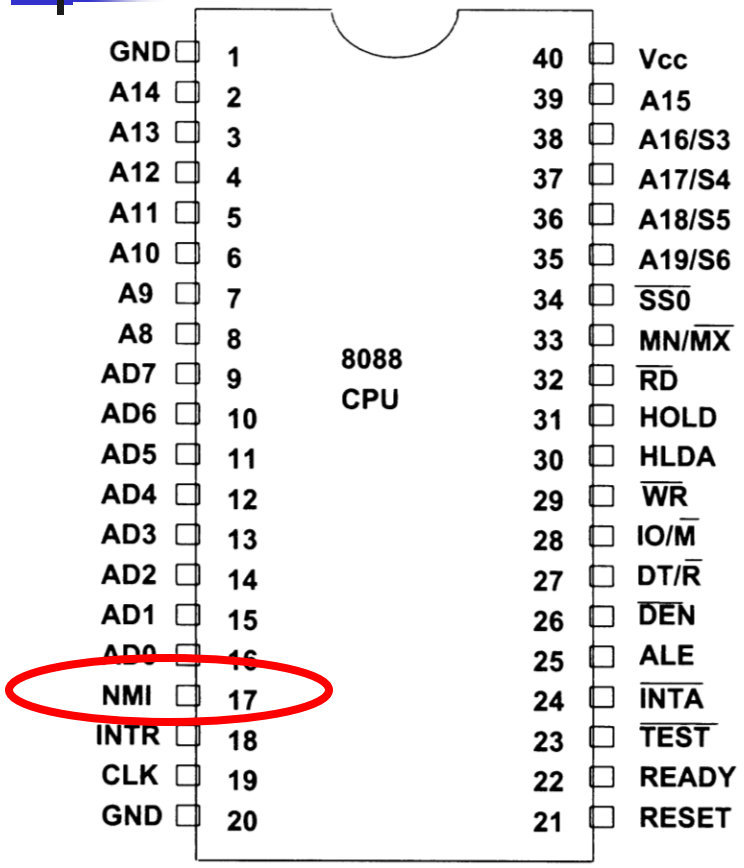


Pin Out Descriptions



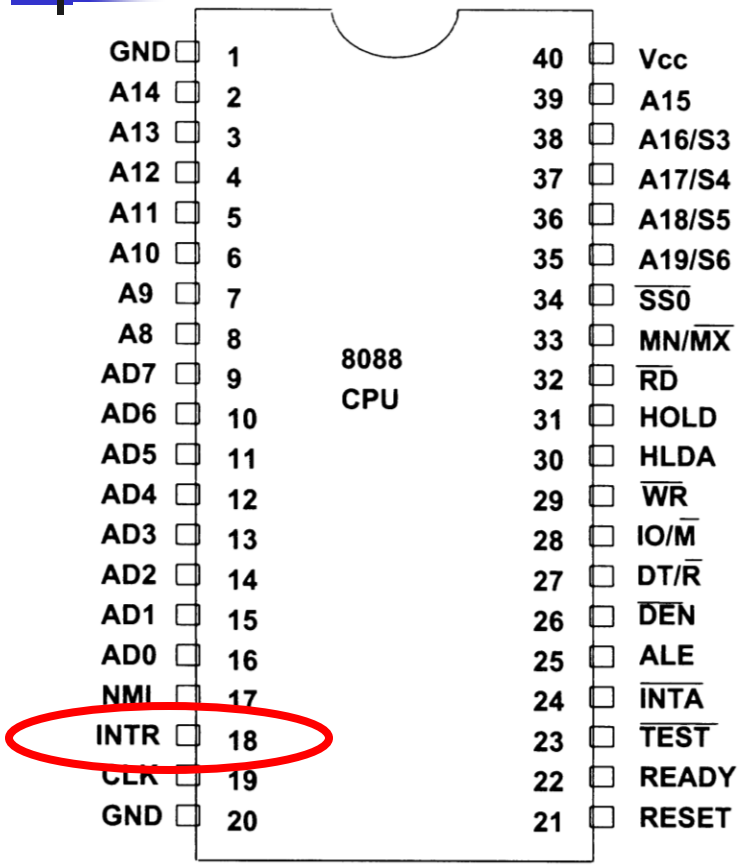
- $\overline{\text{BHE}}$
- Bus High Enable
- Distinguishes between upper and lower bytes of a word
- Only on 8086

Pin Out Descriptions



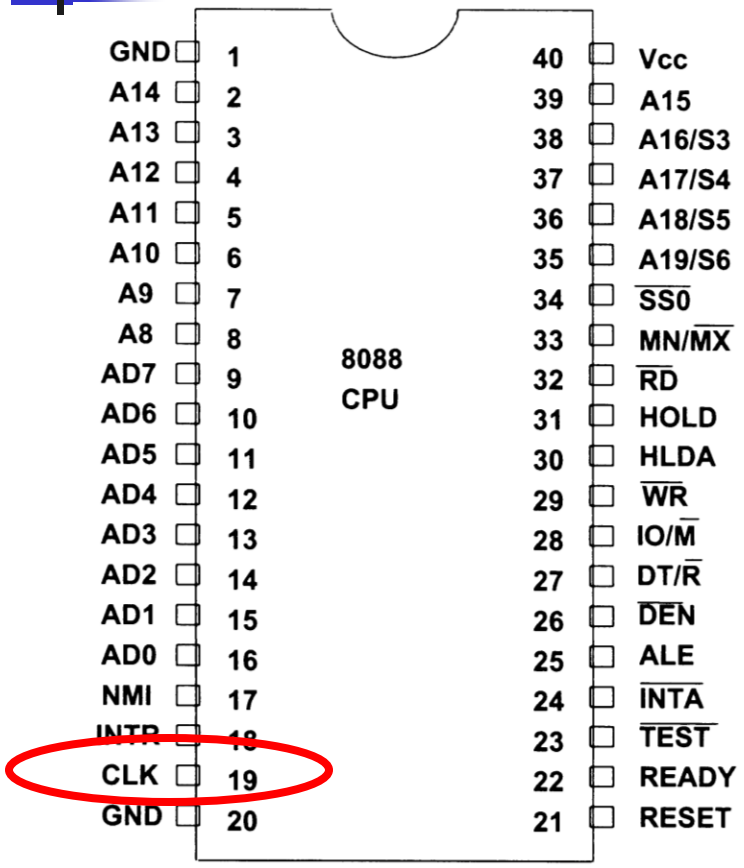
- NMI
- Non Maskable Interrupt
- Input signal
- Causes a jump to the vector table after execution of the current instruction ends

Pin Out Descriptions



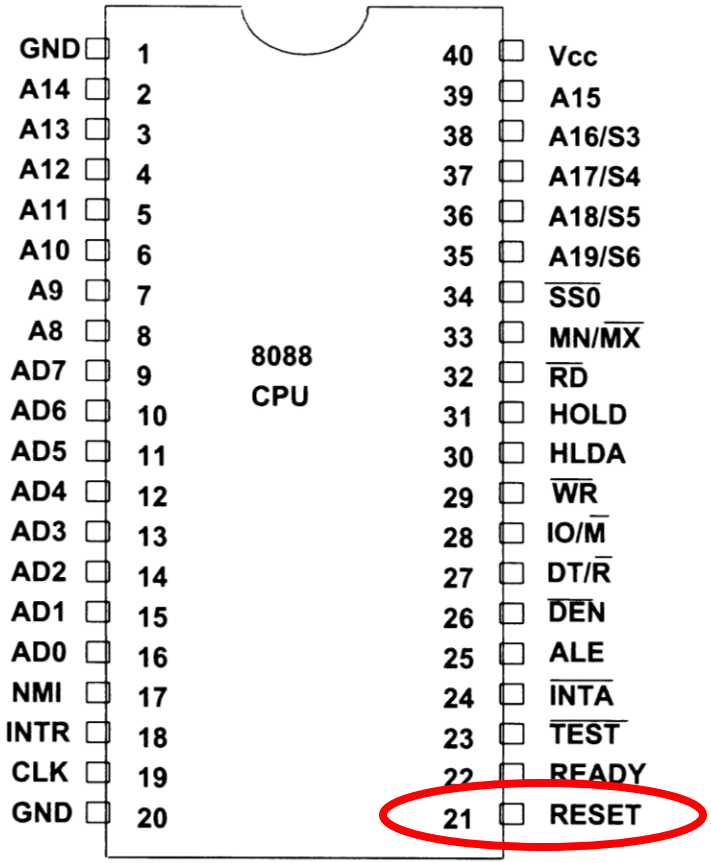
- INTR
- Interrupt Request
- Processor responds with an interrupt acknowledgement after last cycle of current instruction
- Connected to 8259 interrupt controller
- INTA provided by 8288

Pin Out Descriptions



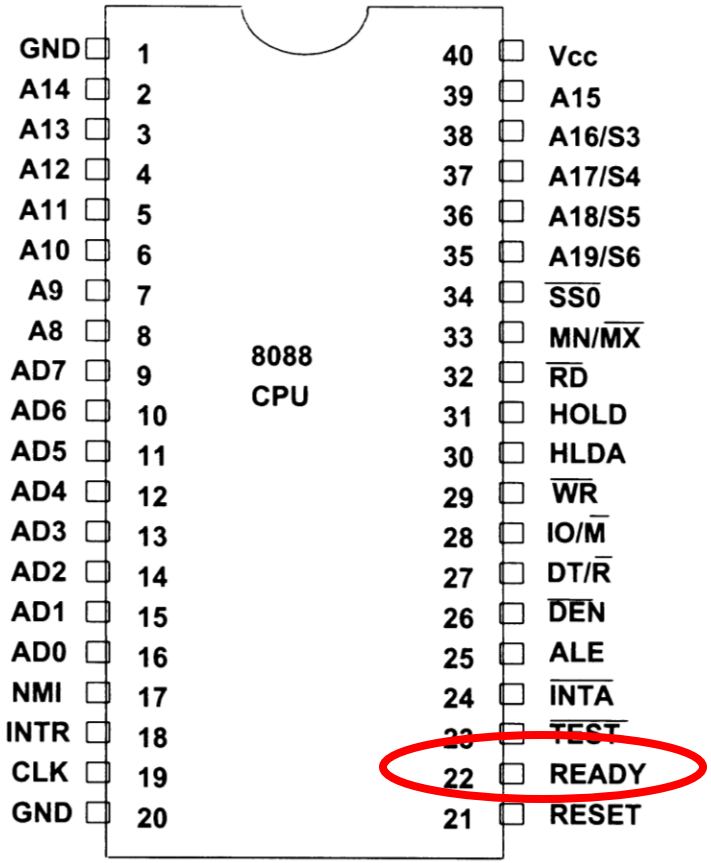
- CLK
- Clock
- Input connected to 8284 clock generator

Pin Out Descriptions



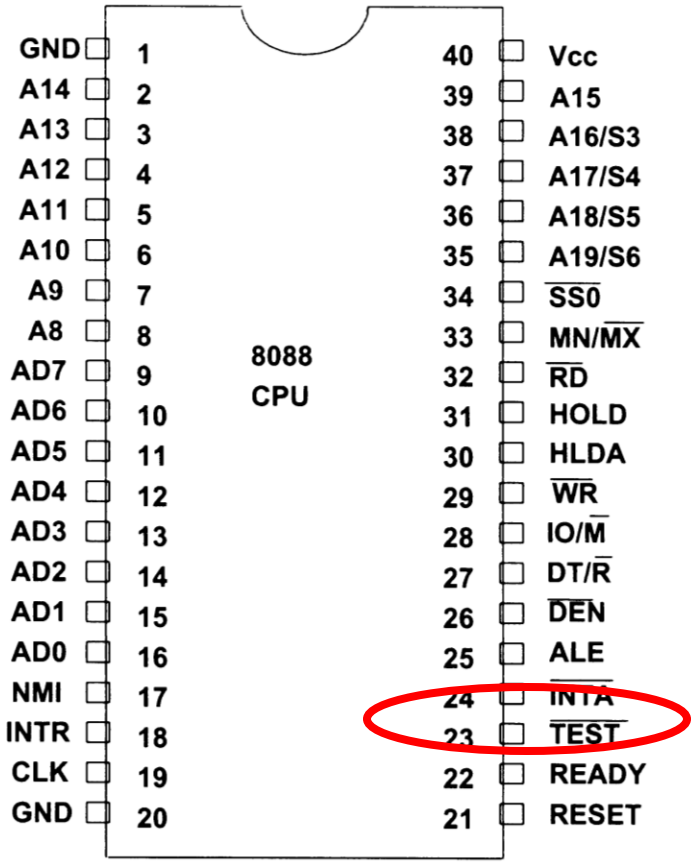
- RESET
- Terminates present activities and discards everything
- After reset
  - CS=FFFFH
  - DS=0000H
  - SS=0000H
  - ES=0000H
  - IP=0000H
  - Flags cleared
  - Queue empty

Pin Out Descriptions



- READY
- Inserts a wait state to handle slower memories when $\overline{\text{READY}}$

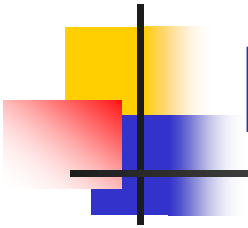
Pin Out Descriptions



- TEST
- Input from the 8087
- Used to synchronize the 8088 and the 8087
- Checked while WAIT instruction executing

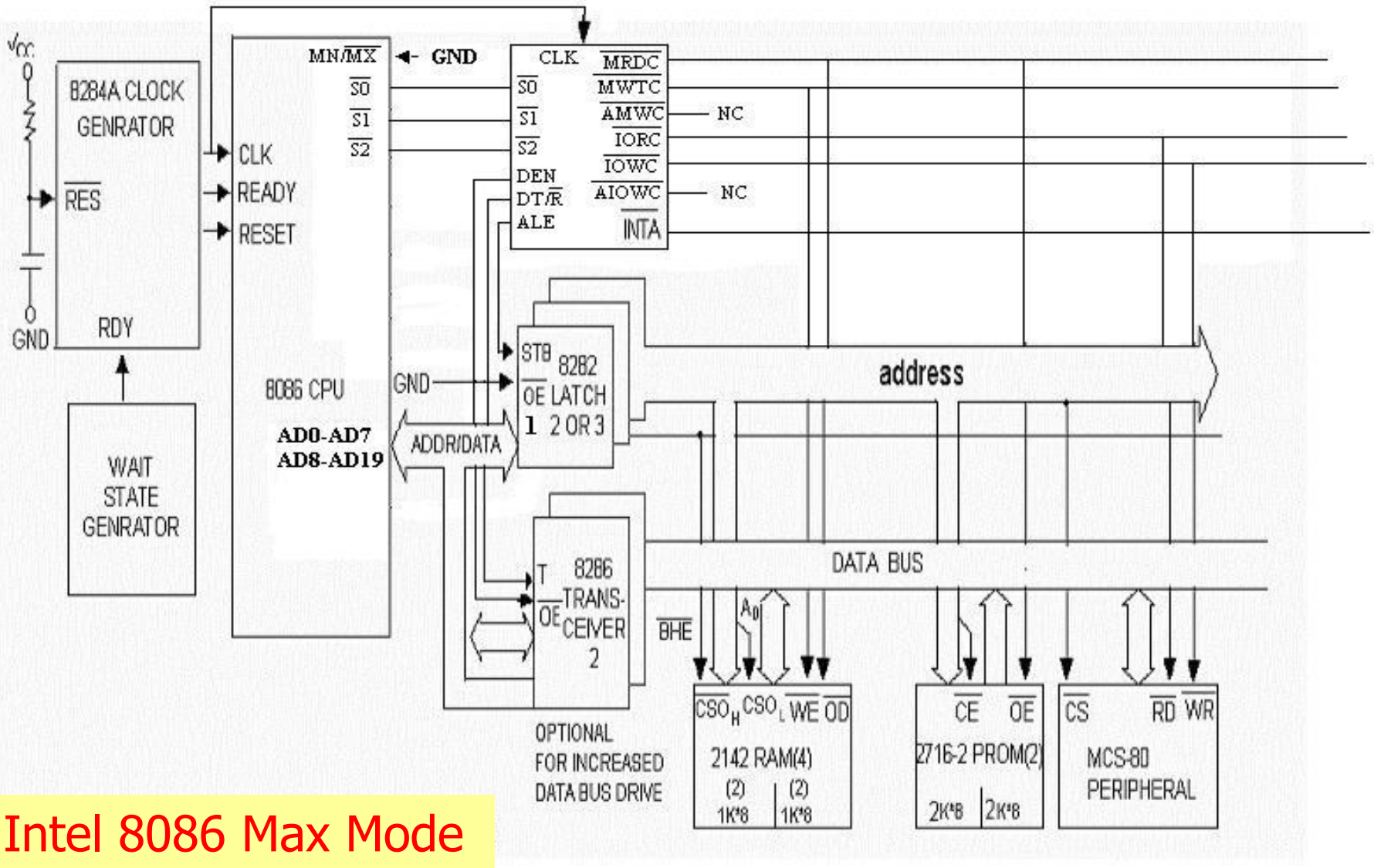
STATUS SIGNALS

- S4,S3 INDICATE SELECTED SEGMENT
  - 00 SUPLEMENTRY DATA
  - 01 STACK
  - 10 CODE SEGMENT
  - 11 DATA SEGMENT
- S5 IS COPY OF INTERRUPT ENABLE FLAG
- S6 8086 IS BUS MASTER (ZERO)
- S7 NOT USED IN 8086



Minimum/Maximum Mode

- Affects functions of pins 24-31
- Minimum Mode
  - Pins 24-31 are memory and I/O control signals
  - Control signals generated internally
  - Similar to 8085A pins
- Maximum Mode
  - Some control signals generated externally
  - Some pins used for new features
  - Must be used when using an 8087

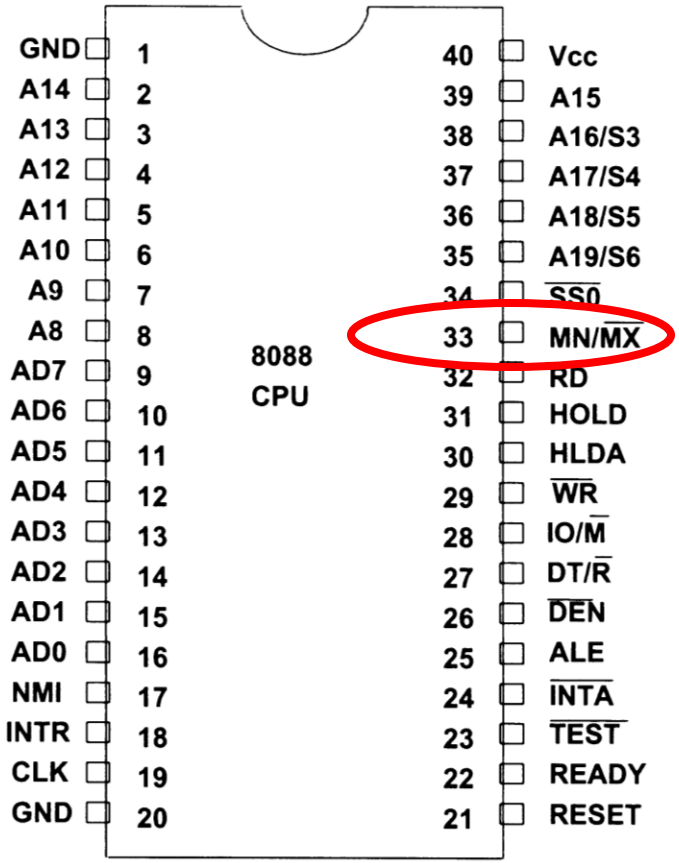


Intel 8086 Max Mode

MIN & MAX MODE SIGNALS

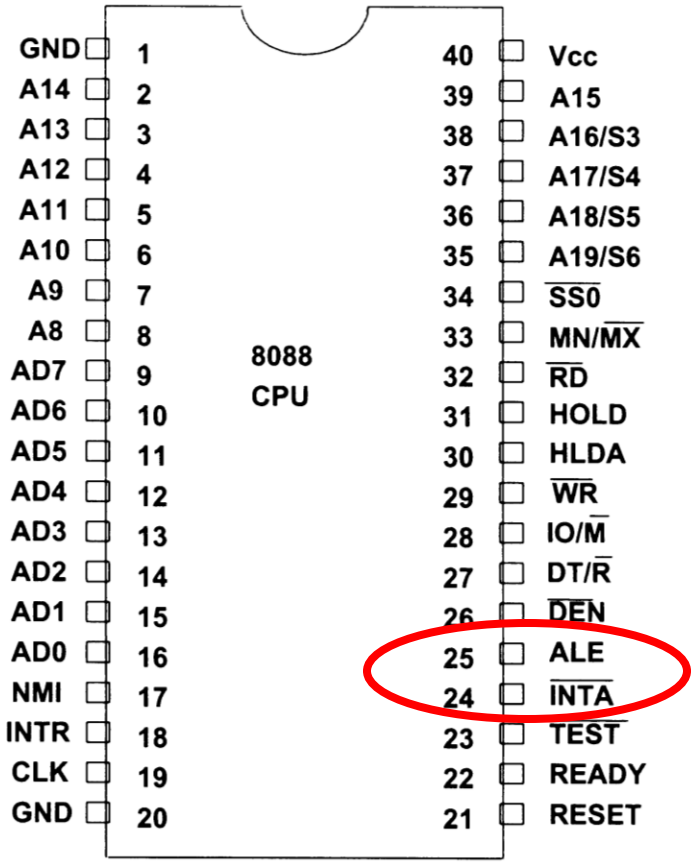
- Min mode Signals
  - $\overline{M}/\overline{IO}$ (28)
  - $\overline{WR}$ (29)
  - $\overline{INTA}$ (24)
  - DT/$\overline{R}$ (27)
  - $\overline{DEN}$ (26
  - ALE (25)
  - HOLD (30)
  - HLDA (31)
- MAX MODE
  - QS1 (24)
  - QS0 (25)
  - SO (26)
  - S1 (27)
  - S2 (28)
  - LOCK (29)
  - RQ/GT1 (30)
  - RQ/GT0 (31)

Pin Out Descriptions



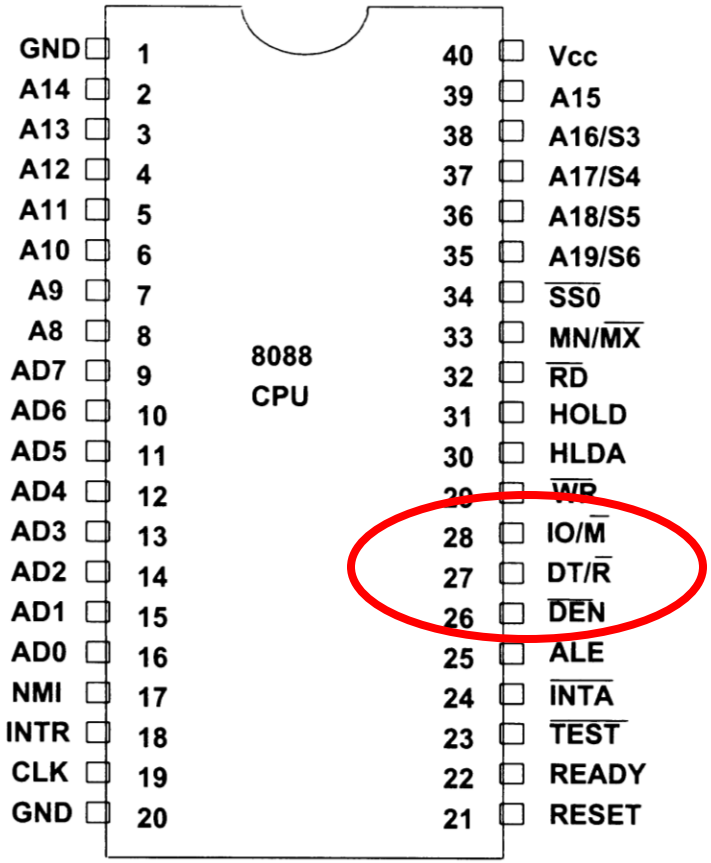
- MN/$\overline{MX}$
- Minimum mode = +5V
- Maximum mode = Gnd

Pin Out Descriptions – Max



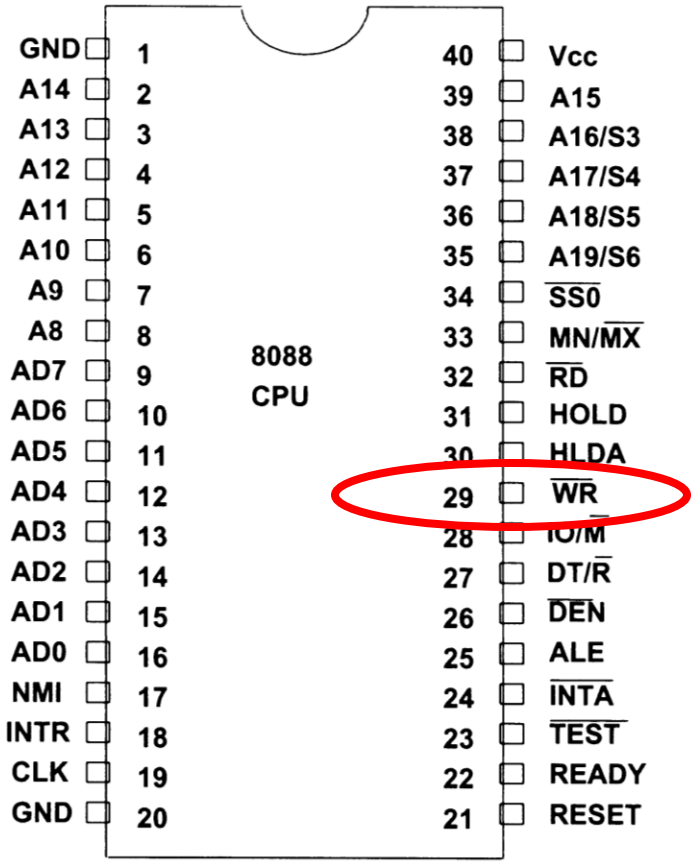
- QS0, QS1
- Queue status
- Status of opcode queue in the processor
  - 00 – No operation
  - 01 – first byte of an instruction has been taken from queue
  - 10 – queue reinitialized (empty
  - 11 – subsequent byte from queue has been taken

Pin Out Descriptions – Max



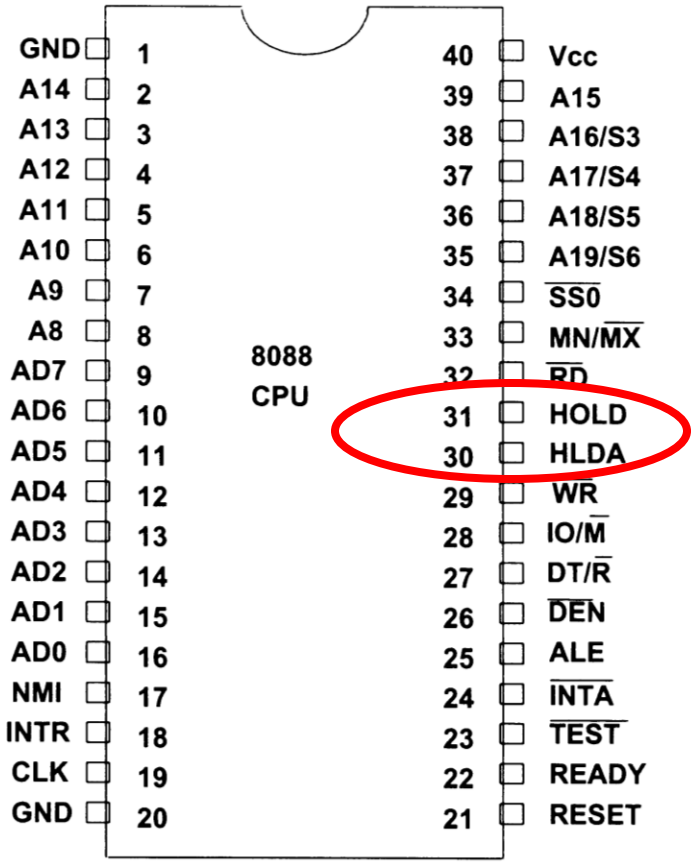
- $\overline{S0}$, $\overline{S1}$, $\overline{S2}$
- Status Signal Pins (S2-S0)
  - 000 – INTA – interrupt acknowledge
  - 001 – IORC – read I/O port
  - 010 – IOWC – write I/O port
  - 011 – none - halt
  - 100 – MRDC – Instruction fetch
  - 101 – MRDC – memory read
  - 110 – MWTC – memory write
  - 111 – none - passive

Pin Out Descriptions – Max



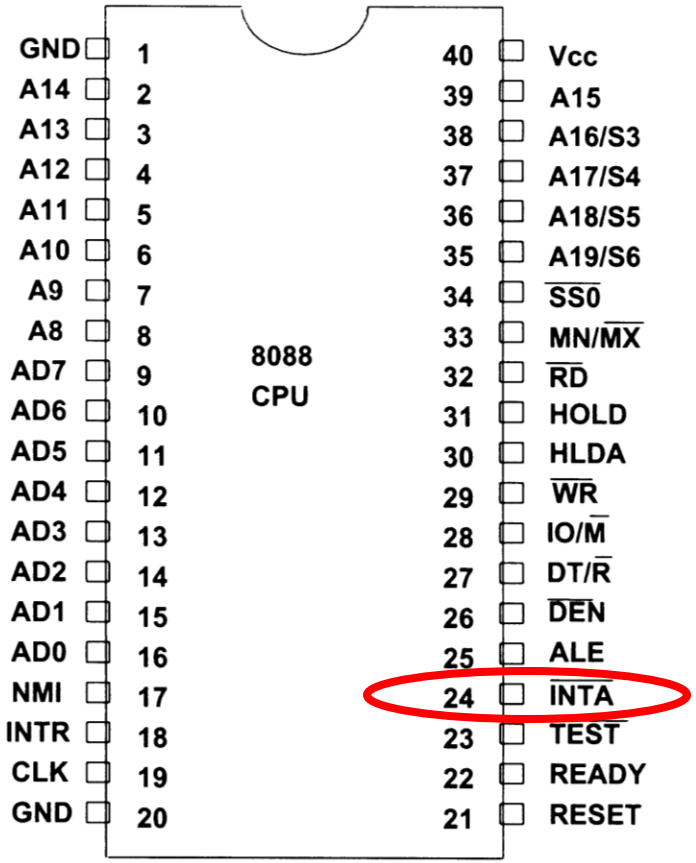
- $\overline{\text{LOCK}}$
- Locks processor to system bus
- Gain the lock by using LOCK prefix on an assembly instruction
- Used with status signals to prevent DMA from gaining control of the buses

Pin Out Descriptions – Max



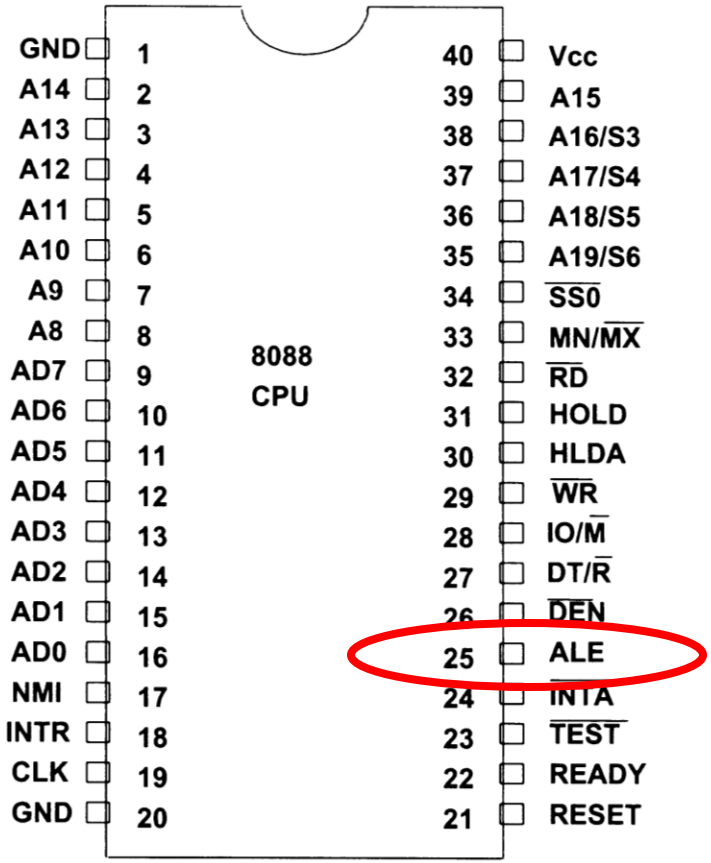
- $\overline{RQ/GT0}$, $\overline{RQ/GT1}$
- Request/Grant
- Bi-directional
- Gain control of local bus
- $\overline{RQ/GT0}$ normally permanently high (disabled)
- $\overline{RQ/GT1}$ is connected to the 8087

Pin Out Descriptions – Min



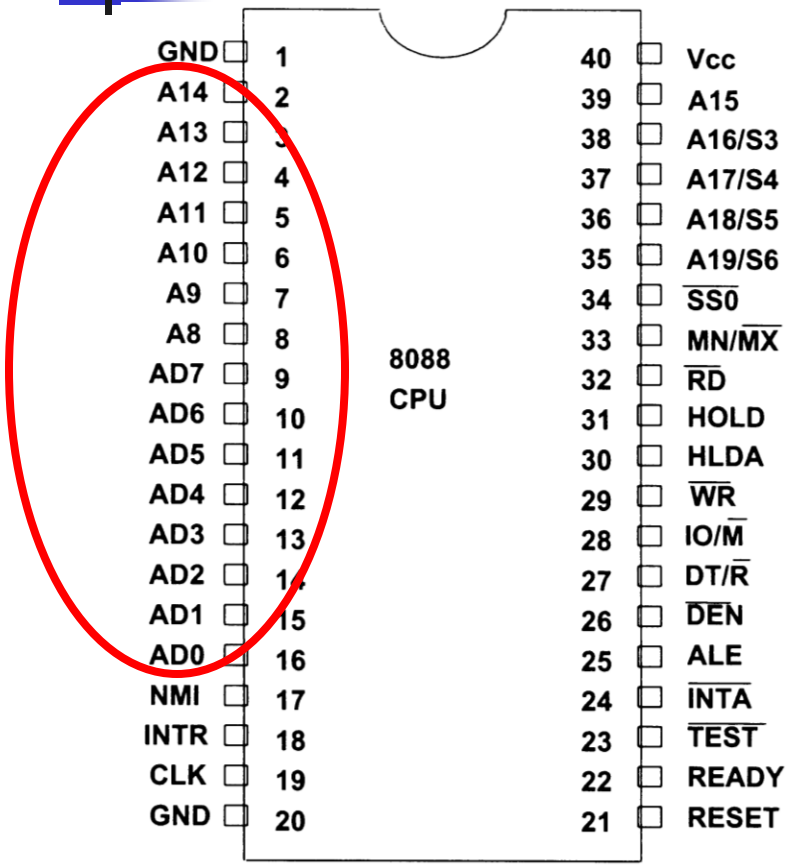
- $\overline{\text{INTA}}$
- Interrupt acknowledge
- Tells interrupt controller that and INTR has occurred and the vector number is on D0-D7

Pin Out Descriptions – Min



- ALE
- Address Latch Enable
- Indicates a valid address on external data bus

Pin Out Descriptions



- AD0-AD15
- Shared address/data lines
- Content determined by ALE

Using the 74LS373 Address Latch

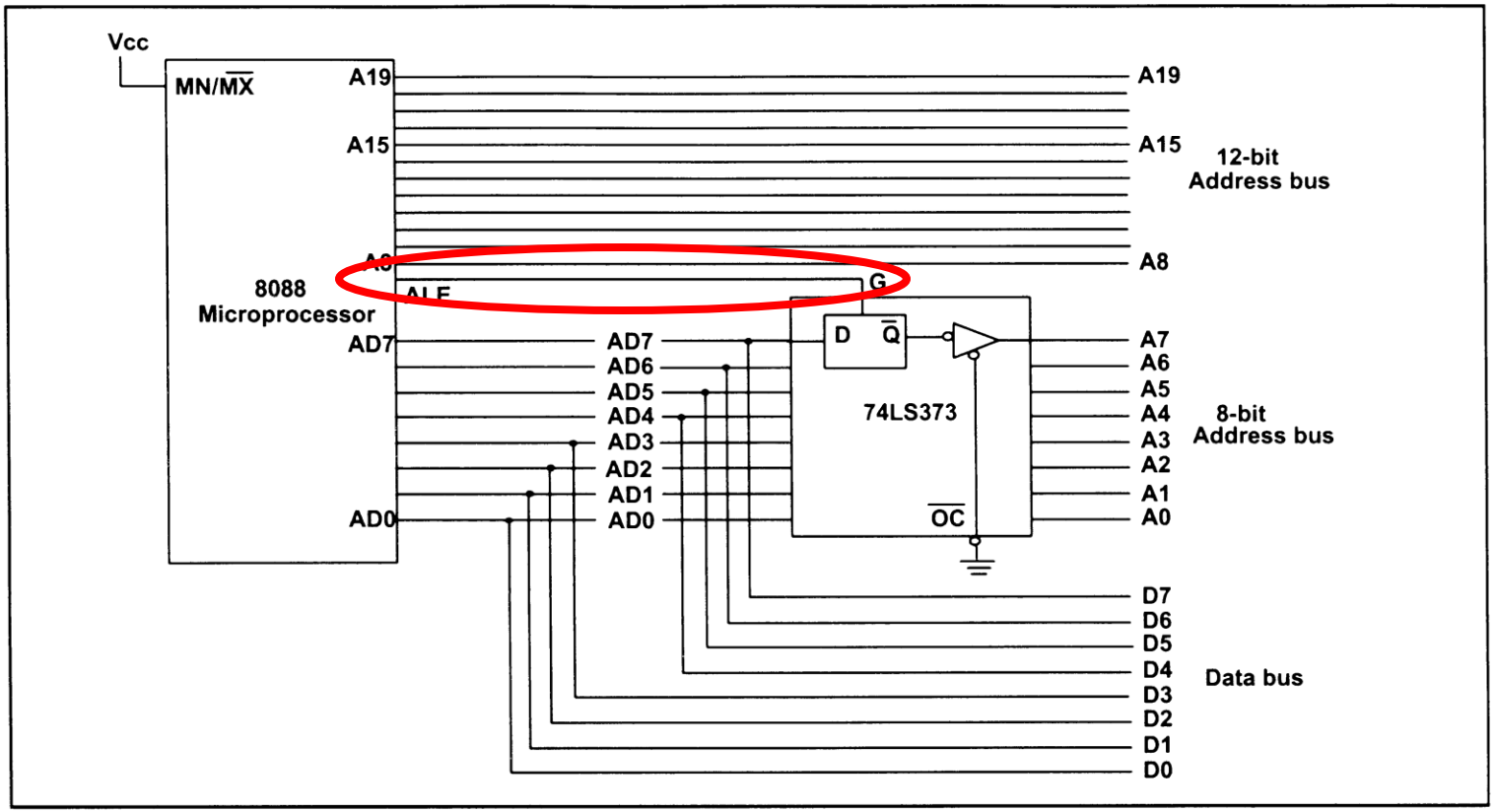
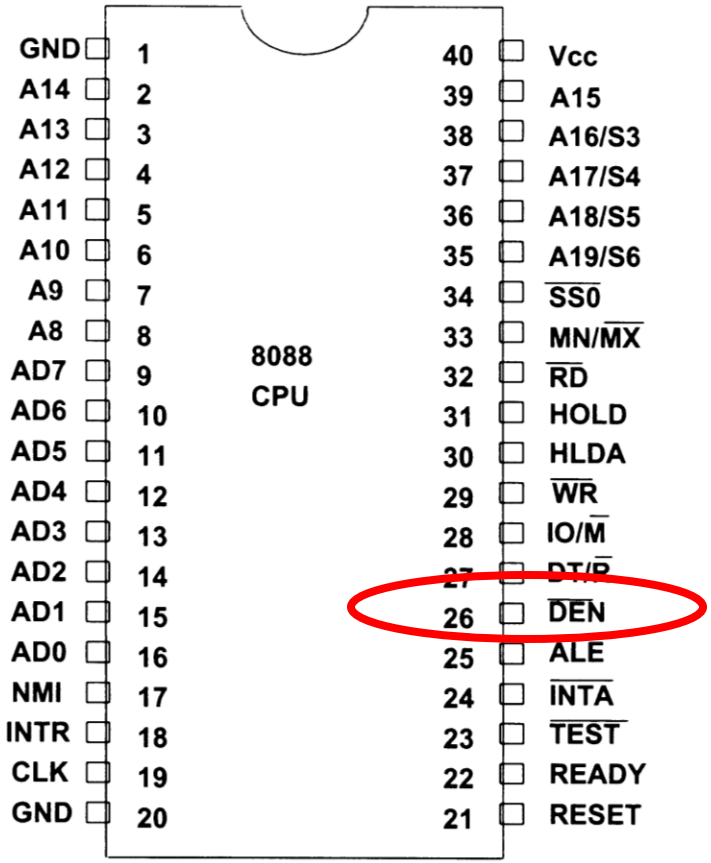


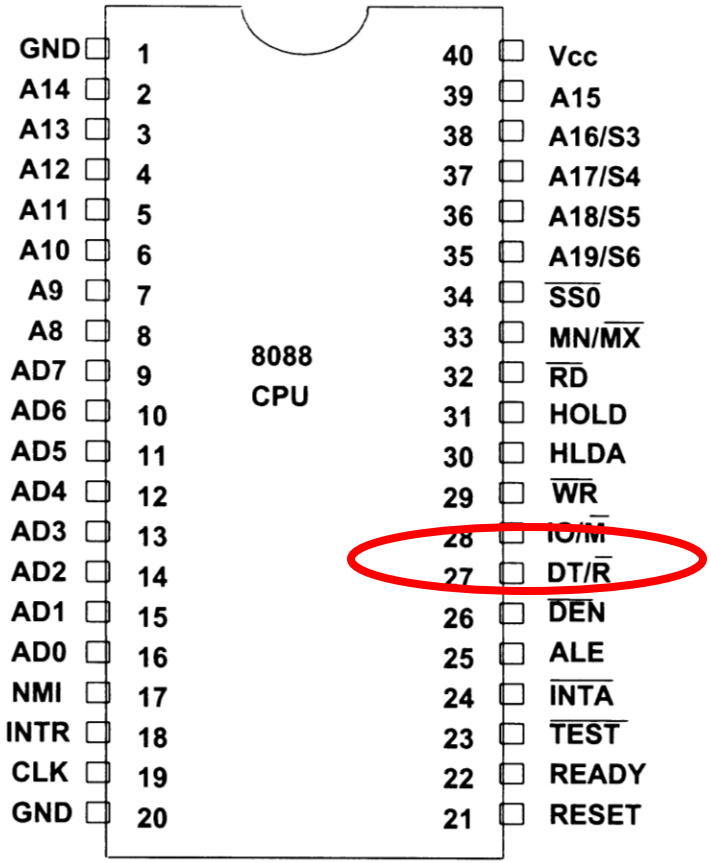
Figure 9-3. Role of ALE in Address/Data Demultiplexing

Pin Out Descriptions – Min



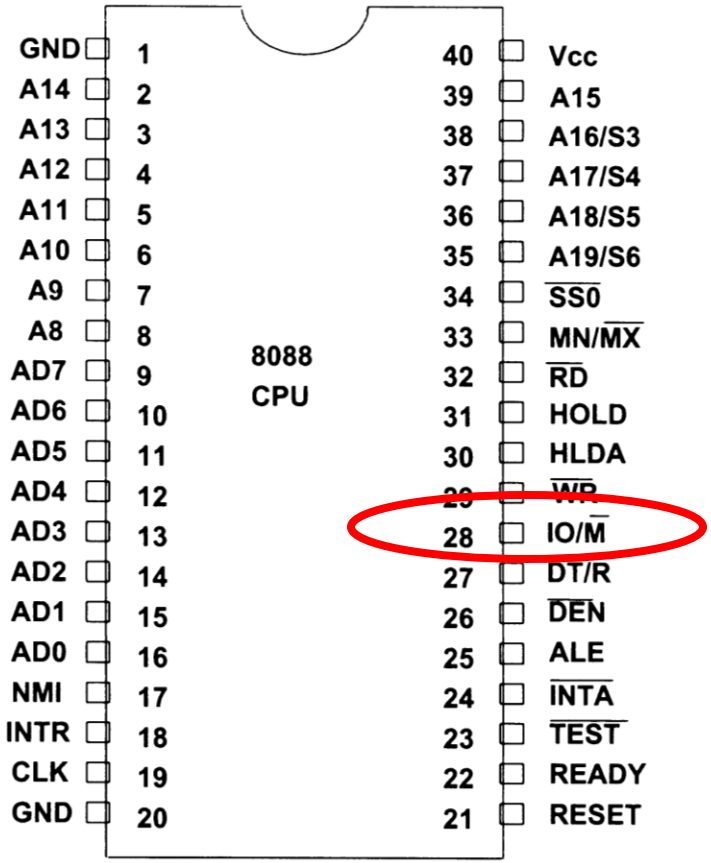
- $\overline{DEN}$
- Data Enable
- Enables the 74LS245
- Allows isolation of CPU from system bus

Pin Out Descriptions – Min



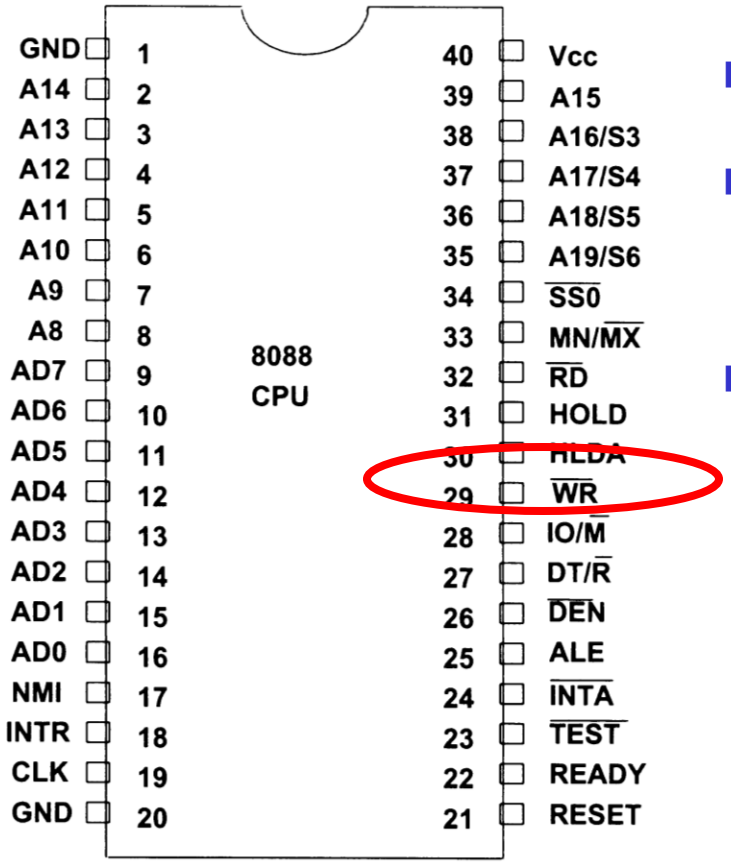
- DT/$\overline{R}$
- Controls direction of data flow through 74LS245 Transceiver

Pin Out Descriptions – Min



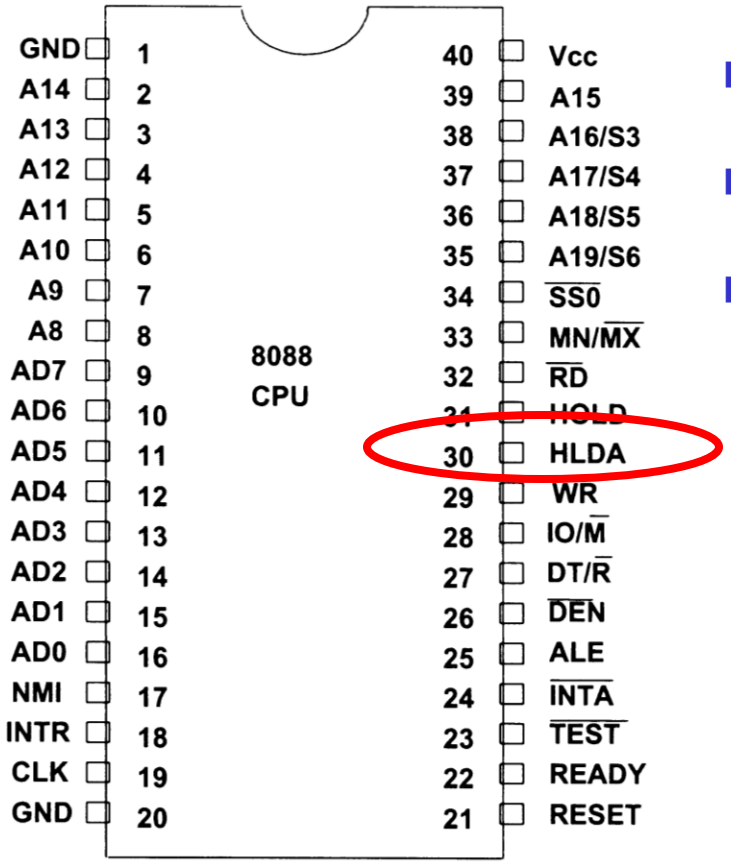
- IO/$\overline{M}$ (8088) or $\overline{IO}$/M (8086)
- Address buss accessing memory or I/O device
- 8088 – low when memory
  - compatible with 8085
- 8086 – high when memory

Pin Out Descriptions – Min



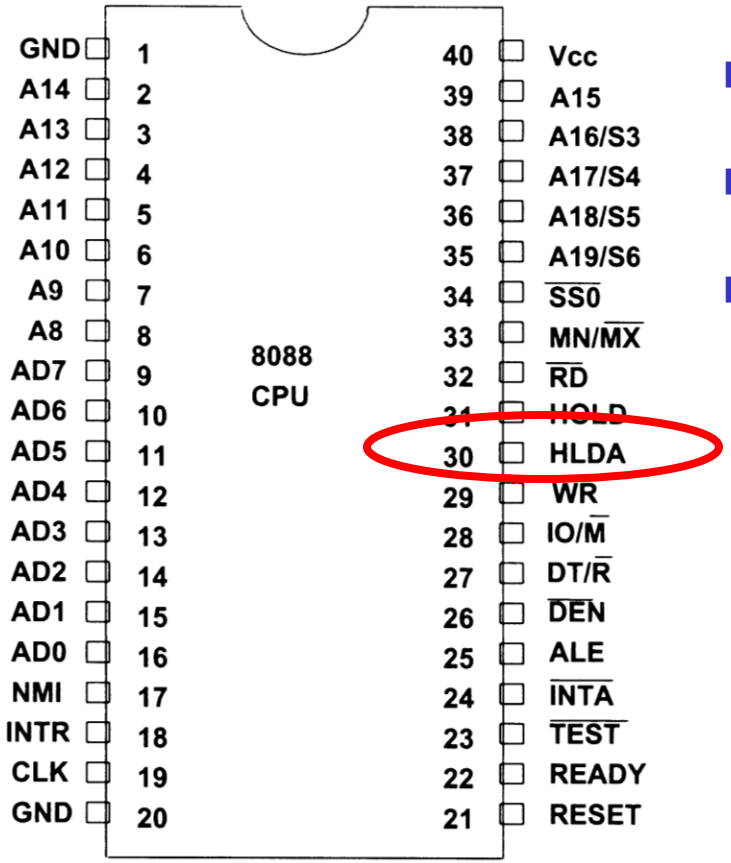
- $\overline{WR}$
- Data on data bus for memory or I/O
- Used with Pin 28 for writes

Pin Out Descriptions – Min



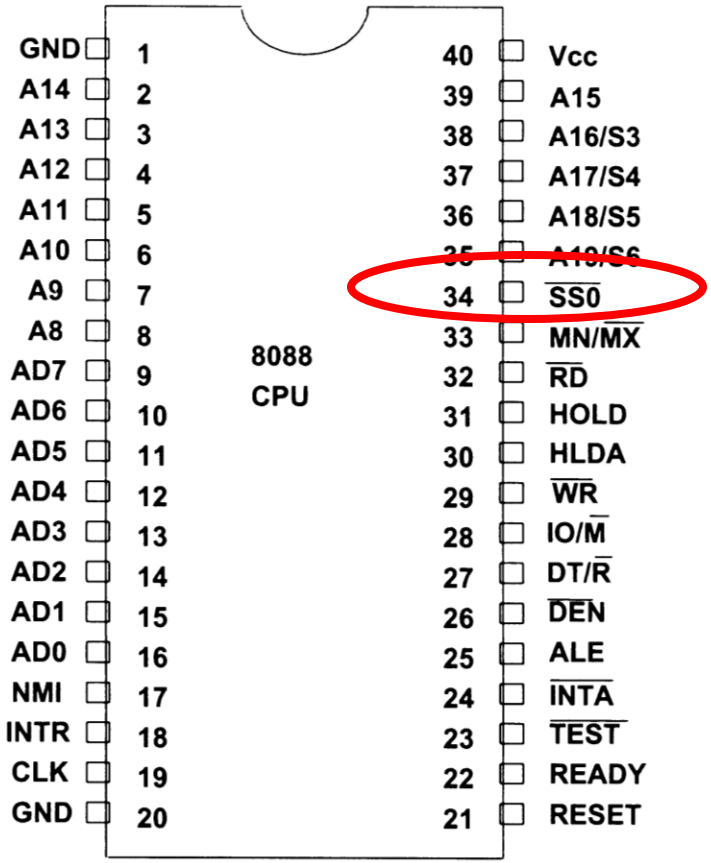
- $\overline{\text{HLDA}}$
- Hold Acknowledge
- Input on HOLD causes CPU to respond with HLDA
  - Signals DMA controller is allowed to use buses

Pin Out Descriptions – Min



- HOLD
- From DMA Controller
- Requests use of local buses form CPU

Pin Out Descriptions – Min



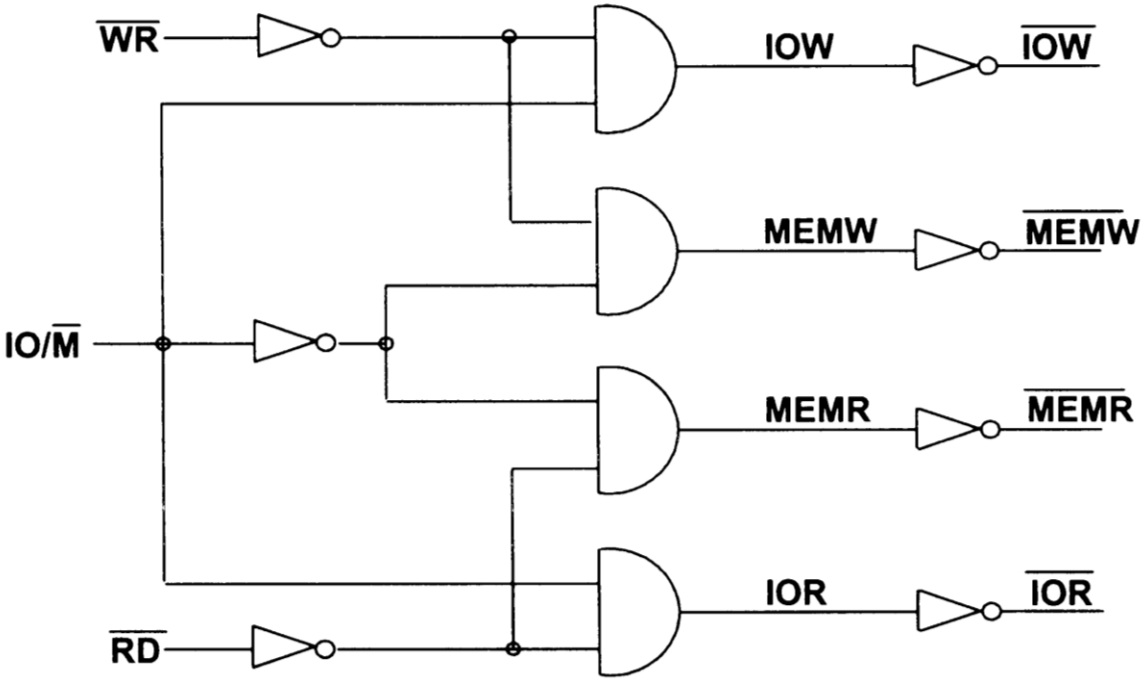
- $\overline{SSO}$
- 8088 only
- Used with IO/M and DT/R to decode status of current bus cycle

Minimum Mode Bus Design

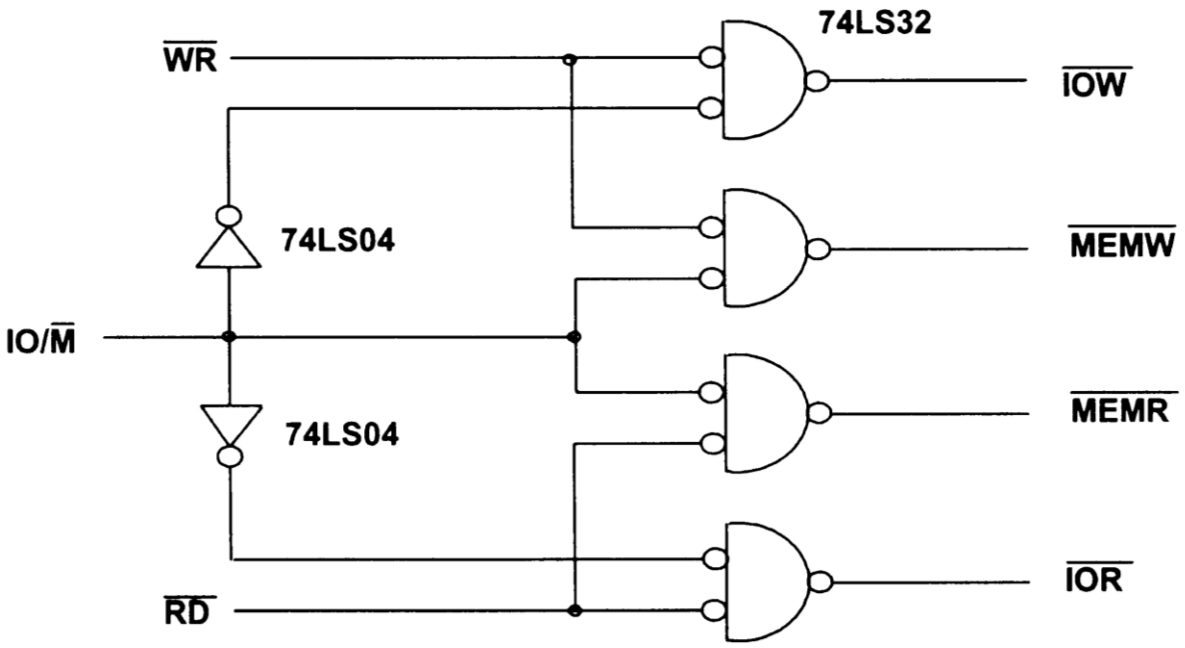
- Some control signals need logic gates
  - Provided by maximum mode
  - 3 Signals provided
    - $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$
    - Generate others

$\overline{RD}$	$\overline{WR}$	IO/$\overline{M}$	Signal
0	1	0	$\overline{MEMR}$
1	0	0	$\overline{MEMW}$
0	1	1	$\overline{IOR}$
1	0	1	$\overline{IOW}$
0	0	X	Never happens

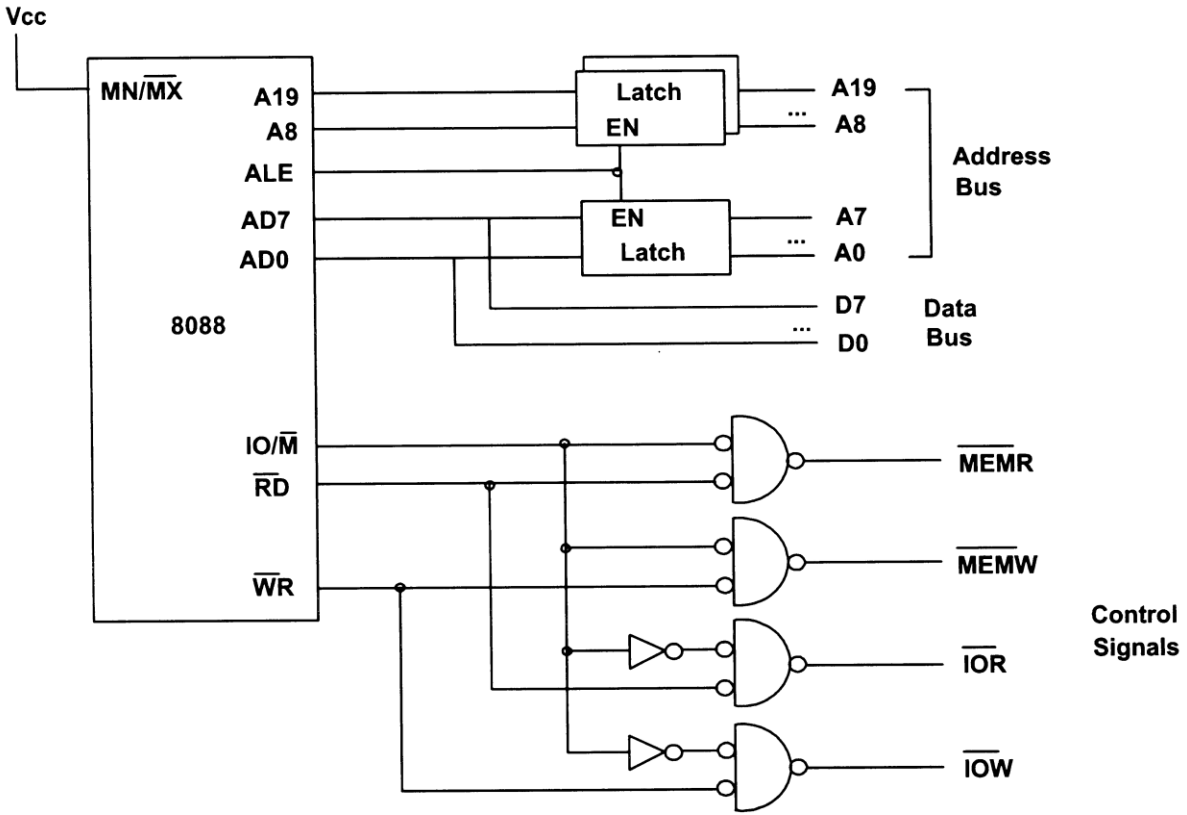
Control Signal Generation (Min Mode)

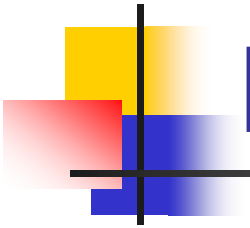


Control Signal Generation (Min Mode)



8088 Bus Control – Min Mode





Next Time:

- Read the rest of the chapter:
  - The 8284 Clock Generator & Driver
  - The 8288 Buss Controller
  - XT Buses