DRAM Controller

Features

- Controls Operation of 8K, 16K, 32K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Devices
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated

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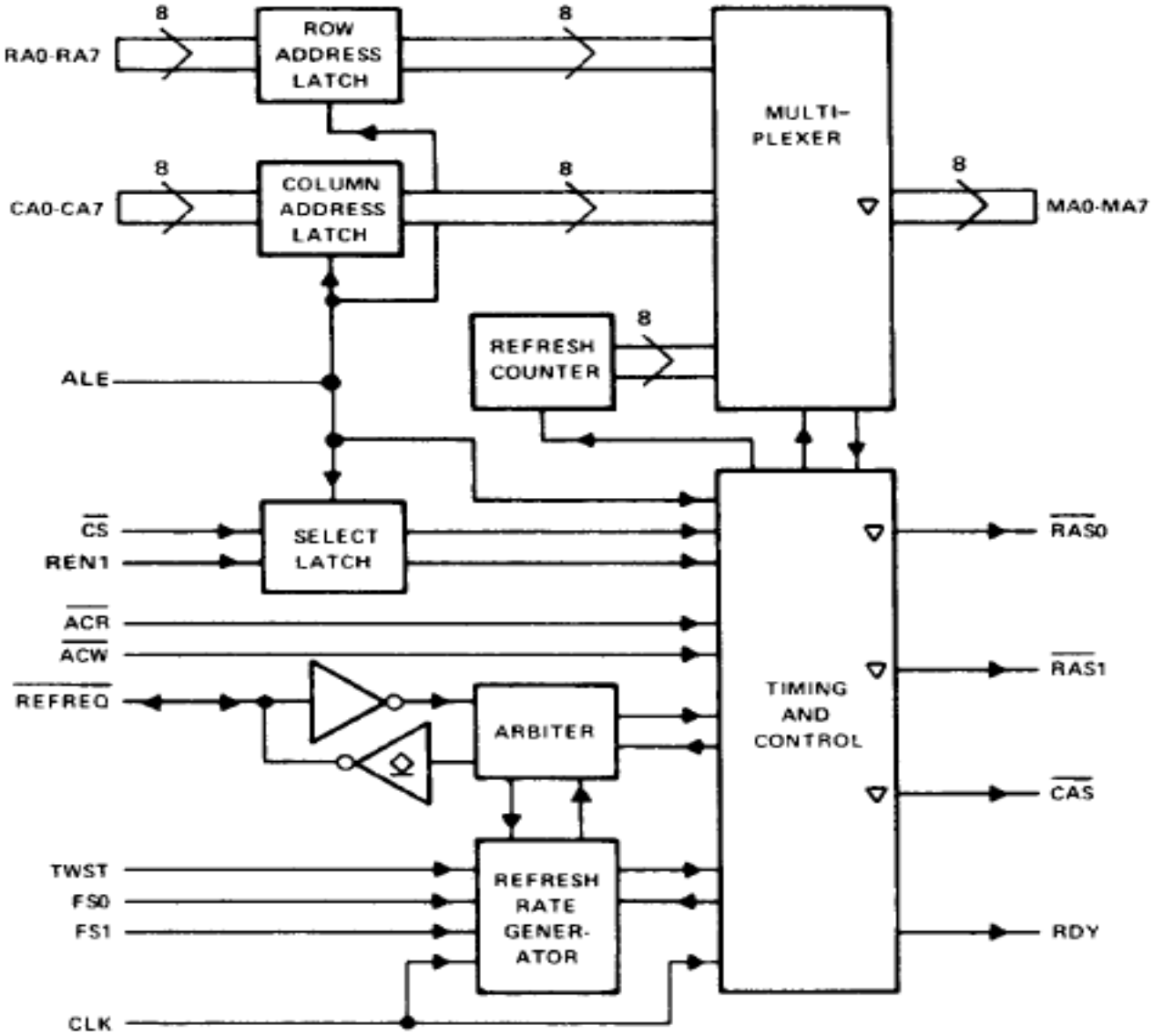
- **Versatile**
  - **Strap-Selected Refresh Rate**
  - **Synchronous, Predictable Refresh**
  - **Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes**
  - **Interfaces Easily to Popular Microprocessors**
- **Strap-Selected Wait-State Generation for Microprocessor/Memory Speed Matching**
- **Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)**
- **3-State Outputs Allow Multiport Memory Configuration**
- **Performance Ranges of 150 ns, 200 ns, or 250 ns**

Functional Block Diagram



The TMS4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing;, control and refresh/accesss arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure date retention.

The TMS4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and 44-pin, 650-mil square plastic carrier package. It is characterized for operation from 0°C to 70°C.