Direct Memory Access & Intel 8237 DMAC

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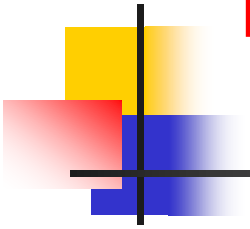
Data Transfer Schemes

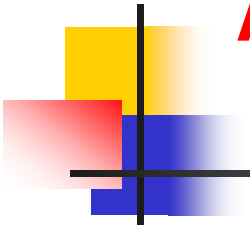


- Programmed I/O
  - Synchronous I/O
  - Asynchronous I/O
  - Interrupt driven I/O
- Direct Memory Access (DMA)

Why DMA

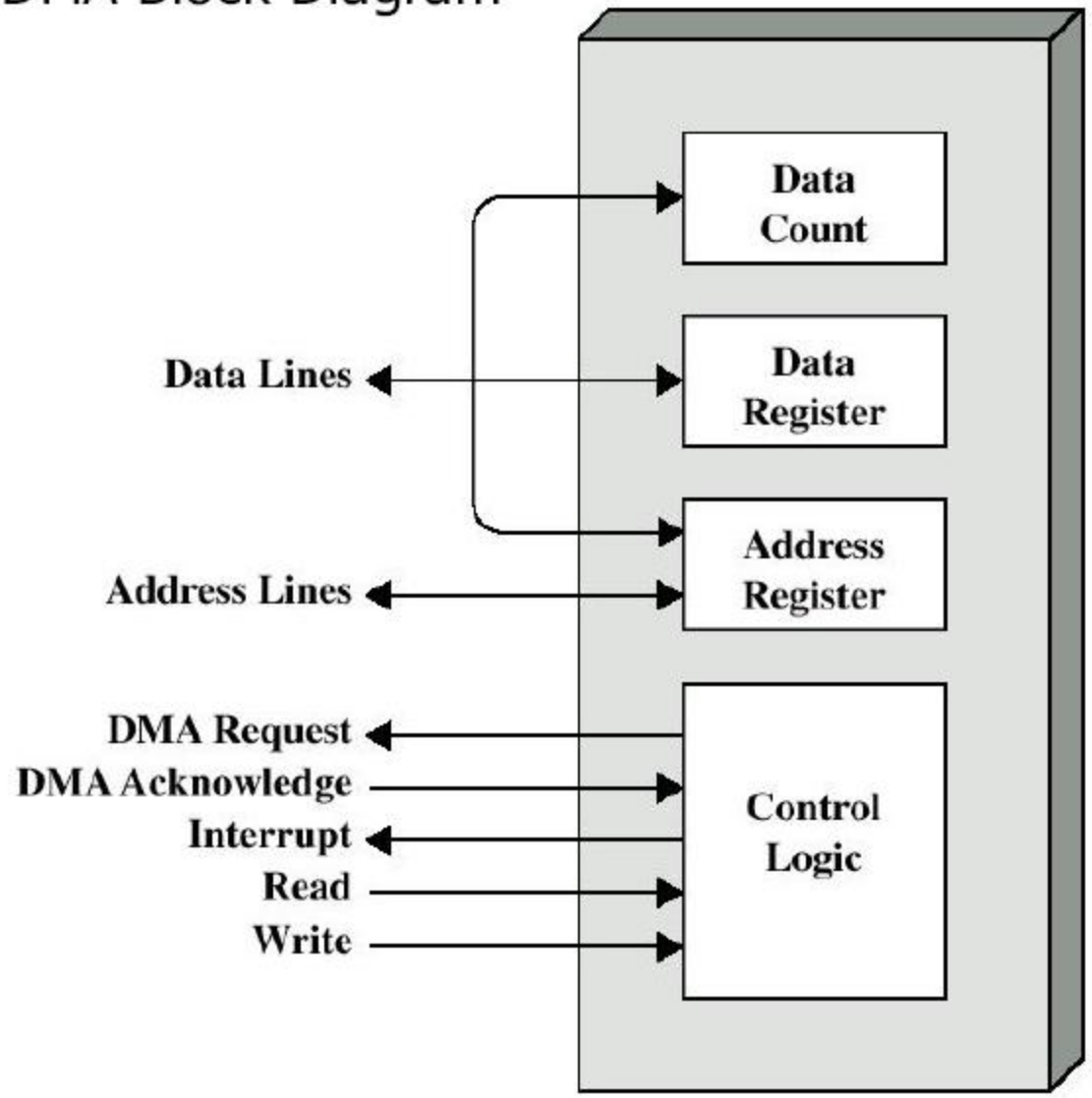
- Interrupt driven and programmed I/O require active CPU intervention
  - —Transfer rate is limited
  - —CPU is tied up in managing an I/O transfer
- When large volumes of data are to be moved, DMA is the answer
- DMA module
  - —Connected to system bus
  - —Transfer data to and from main memory

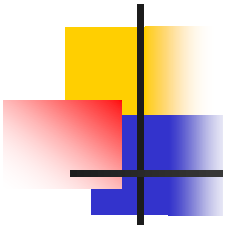
Applications of DMA



- DRAM Refreshing
- Video Display Screen Refreshing
- Bulk data Transfer
  - I/O DEVICES TO MEMORY & MEMORY TO I/O DEVICES TRANSFER
  - MEMORY TO MEMORY DATA TRANSFER

Typical DMA Block Diagram

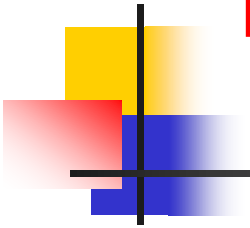




Direct Memory Access

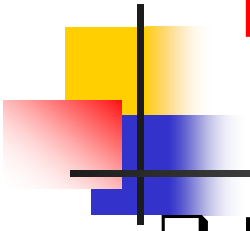
- CPU issues a command to DMA module
  - —Read or write?
  - —Address of the I/O device involved
  - —Starting location in memory
  - —Number of words to be read or written
- CPU continues with other work
  - —An interrupt is sent when the task is complete
  - —CPU is involved only at the beginning and end of the transfer

Features of Intel 8237 DMAC



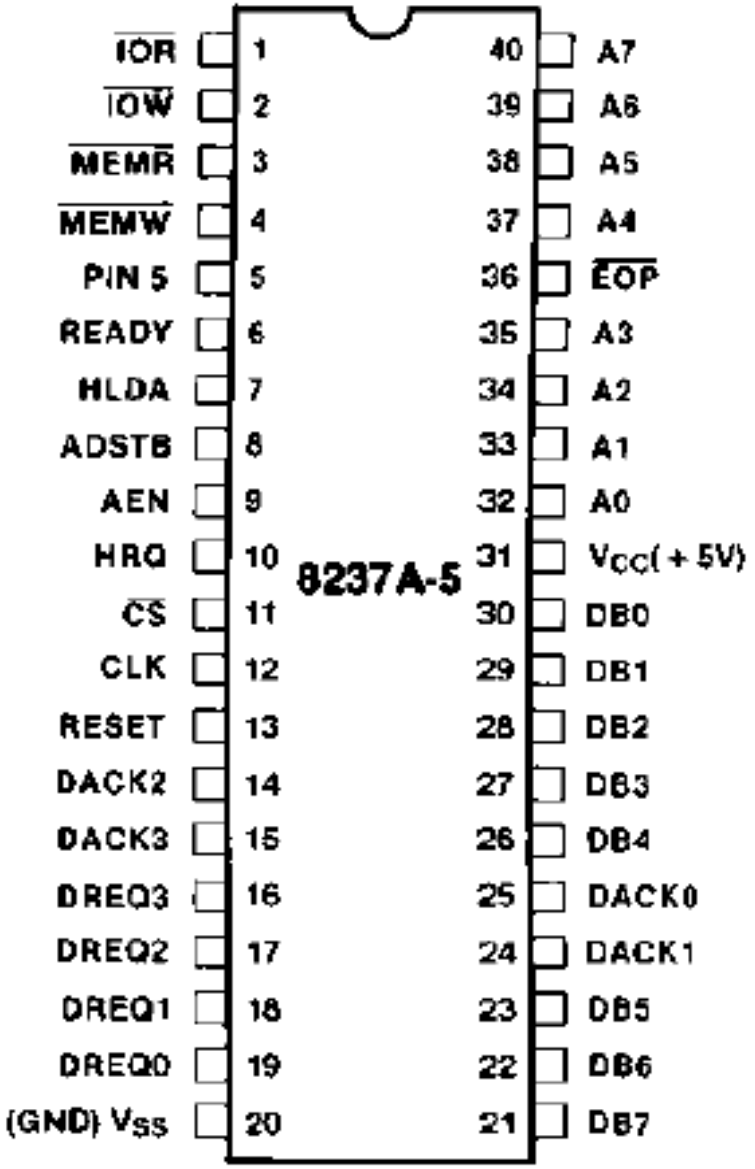
- Enable/Disable Control of Individual DMA Requests
- Four Independent DMA Channels
- Independent Autoinitialization of All Channels
- Memory-to-Memory Transfers
- Memory Block Initialization
- Address Increment or Decrement
- High Performance: Transfers up to 1.6M Bytes/Second with 5 MHz 8237A-5

Features of Intel 8237 DMAC



- Directly Expandable to Any Number of Channels
- End of Process Input for Terminating Transfers
- Software DMA Requests
- Independent Polarity Control for DREQ and DACK Signals
- Available in EXPRESS
  - –Standard Temperature Range
- Available in 40-Lead Cerdip and Plastic Packages

PIN Diagram
Intel 8237



Block Diagram of Intel 8237

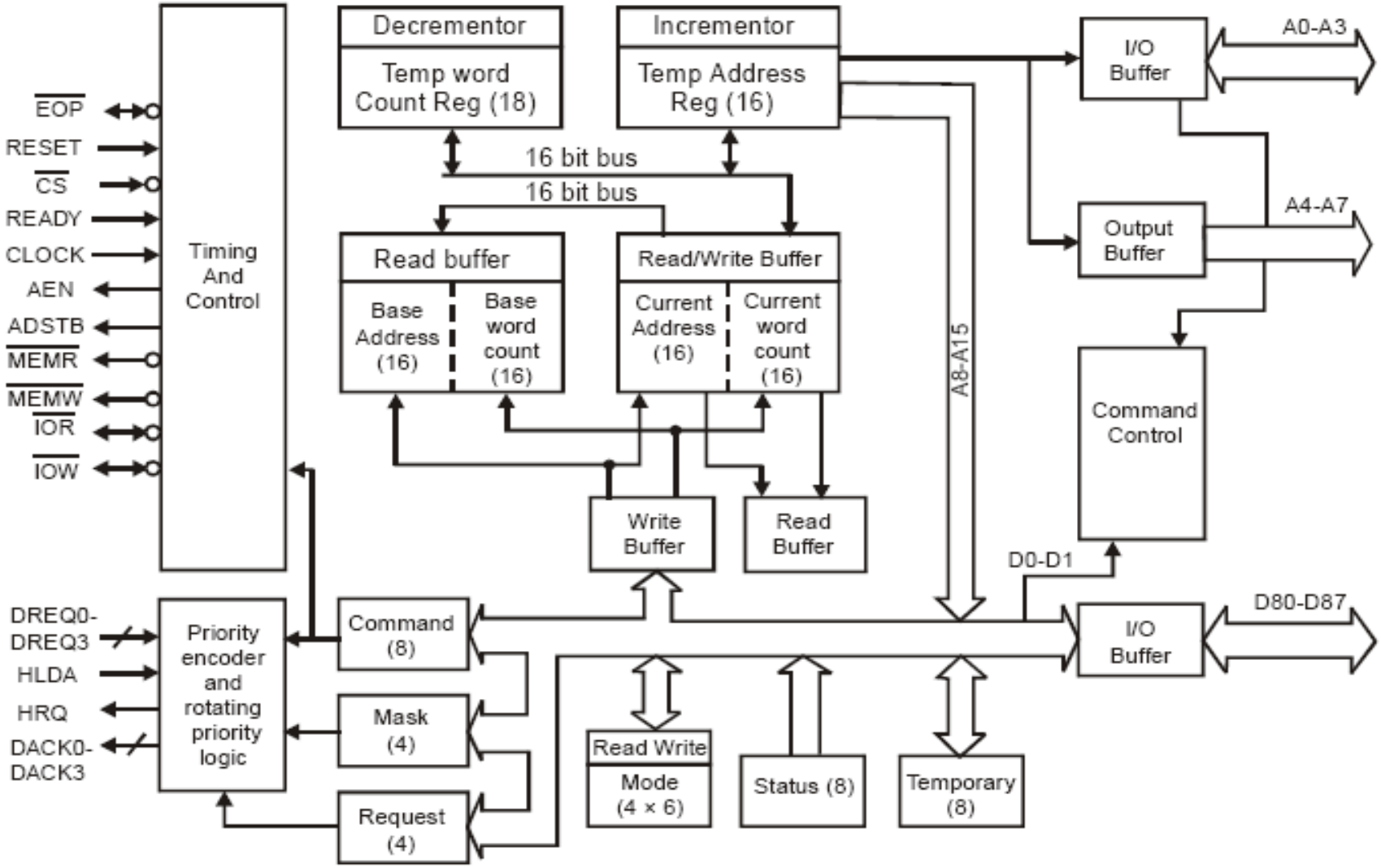


Table 1. Pin Description

Symbol	Type	Name and Function
V_{CC}		**POWER:** +5V supply.
V_{SS}		**GROUND:** Ground.
CLK	I	**CLOCK INPUT:** Clock Input controls the internal operations of the 8237A and its rate of data transfers. The input may be driven at up to 5 MHz for the 8237A-5.
$\overline{CS}$	I	**CHIP SELECT:** Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET	I	**RESET:** Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	**READY:** Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	I	**HOLD ACKNOWLEDGE:** The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.

DREQ0–DREQ3	I	**DMA REQUEST:** The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.

DB0–DB7	I/O	**DATA BUS:** The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237A control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.

$\overline{IOR}$	I/O	**I/O READ:** I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237A to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	I/O	**I/O WRITE:** I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 8237A. In the Active cycle, it is an output control signal used by the 8237A to load data to the peripheral during a DMA Read transfer.

END OF PROCESS: I/O

END OF PROCESS: End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 8237A allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The 8237A also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ line. The reception of $\overline{EOP}$, either internal or external, will cause the 8237A to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.

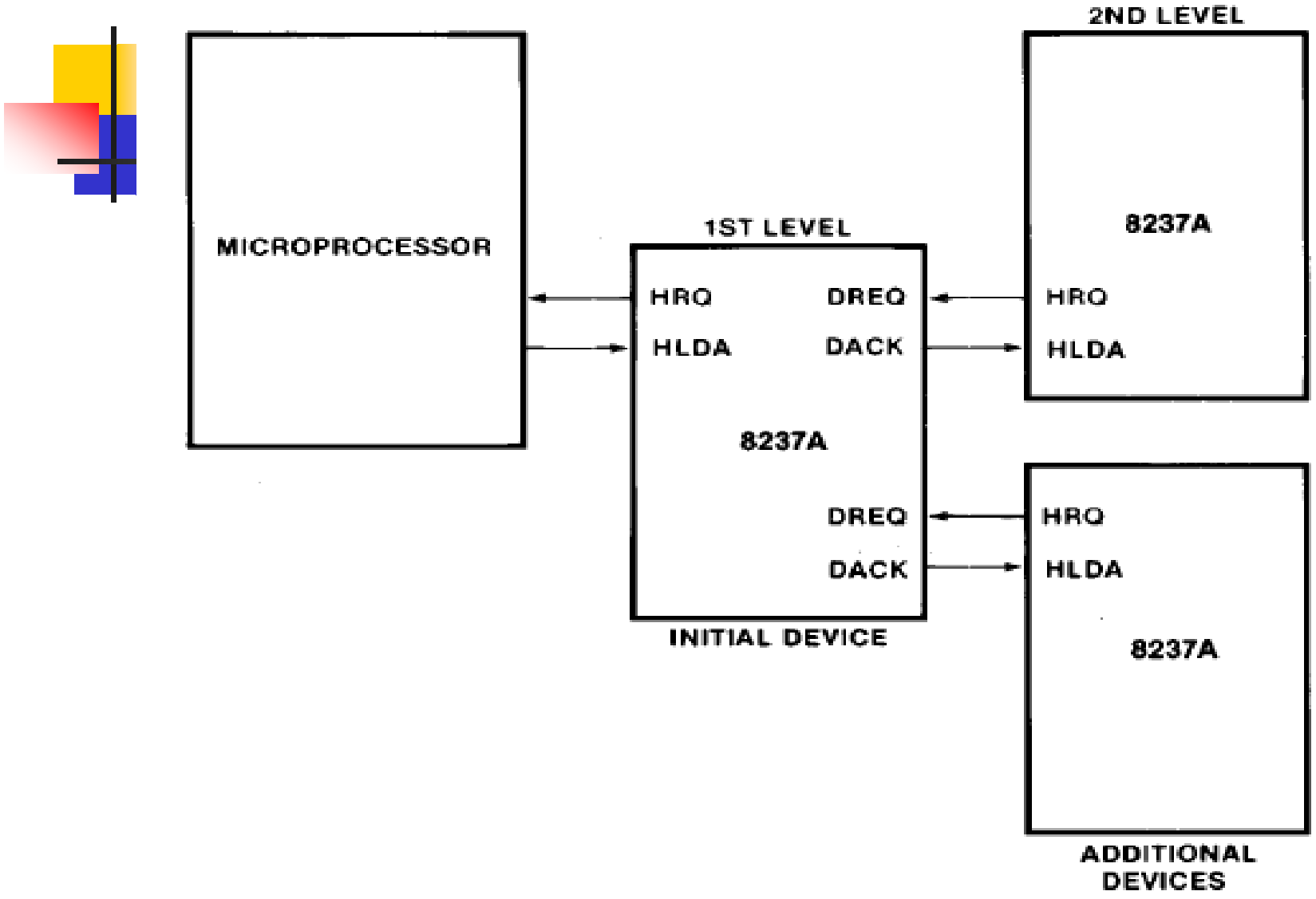
A0–A3	I/O	**ADDRESS:** The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.
A4–A7	O	**ADDRESS:** The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	**HOLD REQUEST:** This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ.

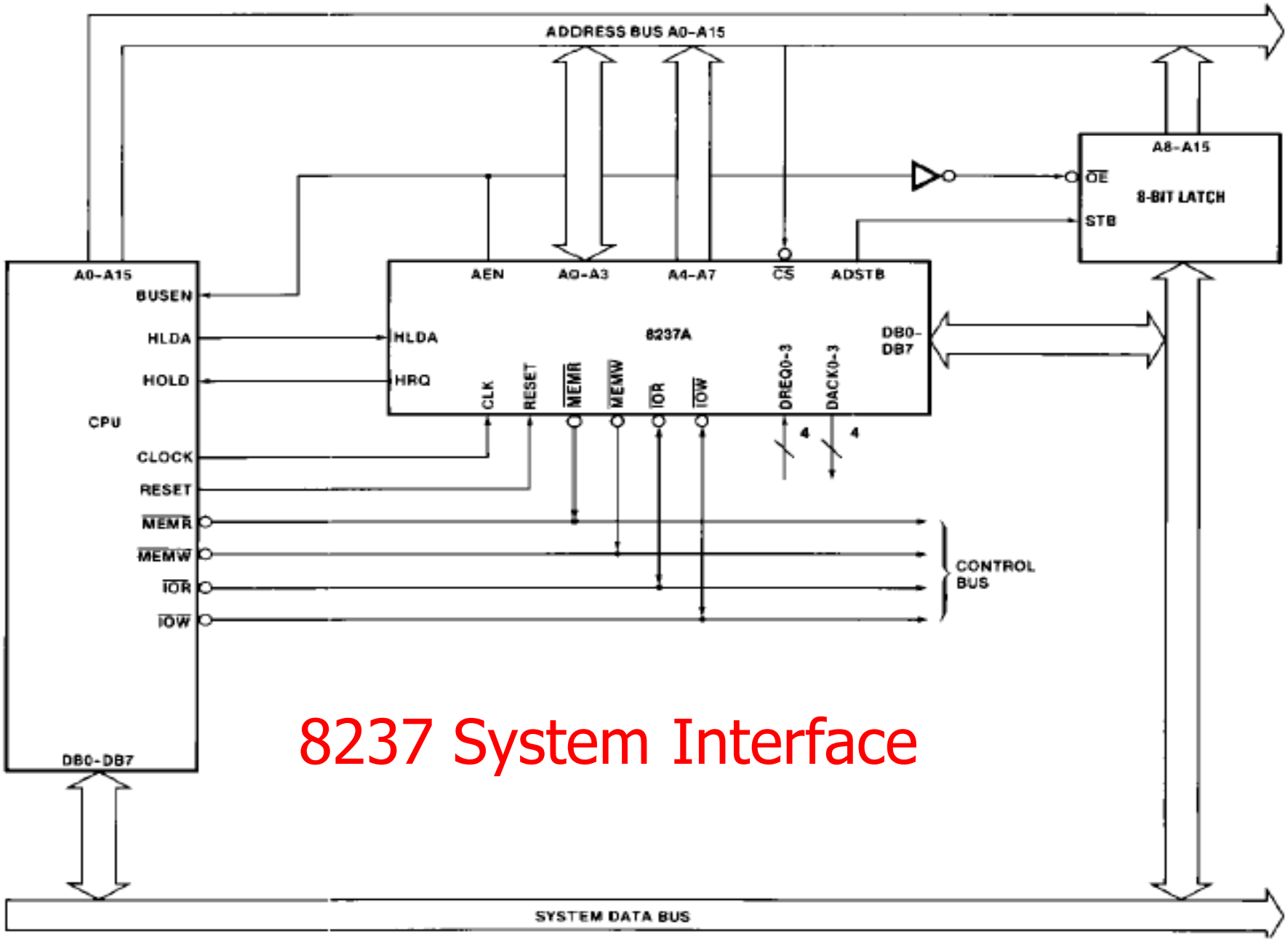
DACK0–DACK3	O	**DMA ACKNOWLEDGE:** DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	**ADDRESS ENABLE:** Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	**ADDRESS STROBE:** The active high, Address Strobe is used to strobe the upper address byte into an external latch.

$\overline{\text{MEMR}}$	O	**MEMORY READ:** The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{\text{MEMW}}$	O	**MEMORY WRITE:** The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.
PIN5	I	**PIN5:** This pin should always be at a logic HIGH level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended however, that PIN5 be connected to V_{CC}.

Internal Registers

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1


2ND LEVEL
MICROPROCESSOR
1ST LEVEL
8237A
HRQ
DREQ
HLDA
DACK
8237A
HRQ
HLDA
DREQ
HRQ
DACK
HLDA
8237A
INITIAL DEVICE
ADDITIONAL
DEVICES



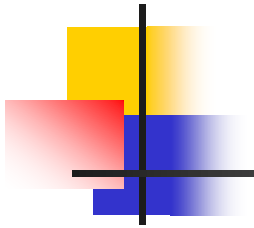
8237 System Interface

PROGRAMMING THE 8237

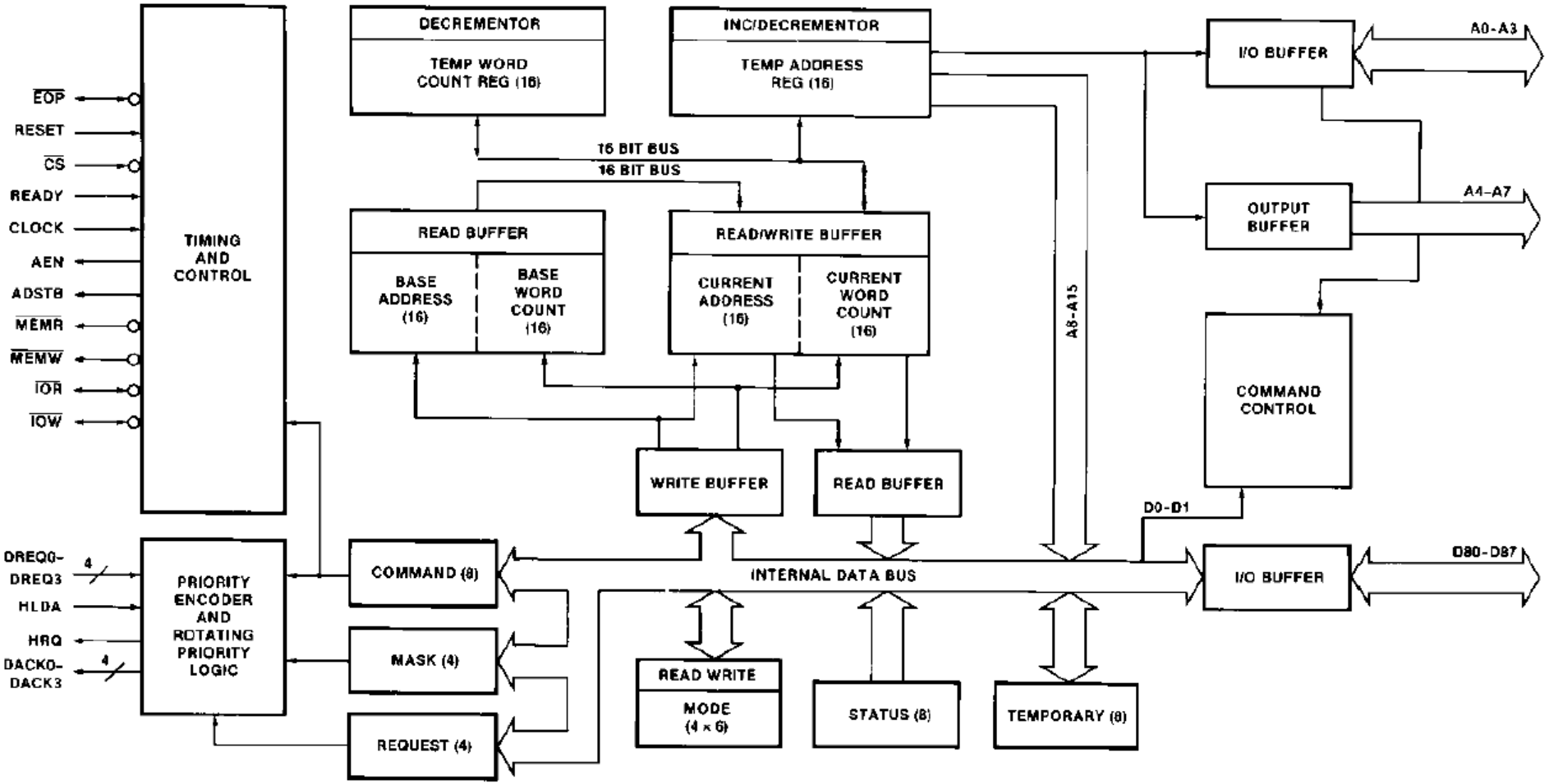
- Write a control word in the mode register that select the channel and specify the type of transfer read,write or verify and the DMA mode (block, single byte etc.)
- Write a control word in the command register that specifies parameters such as priority among four Channels ,DREQ and DACK active levels and timing, and enables the 8237
- Write the starting address of the data block to be transferred in the channel memory address Register(MAR)
- Write the count (the number of the bytes in the data block) in the channel Count register.

DMA EXECUTION (MASTER MODE)

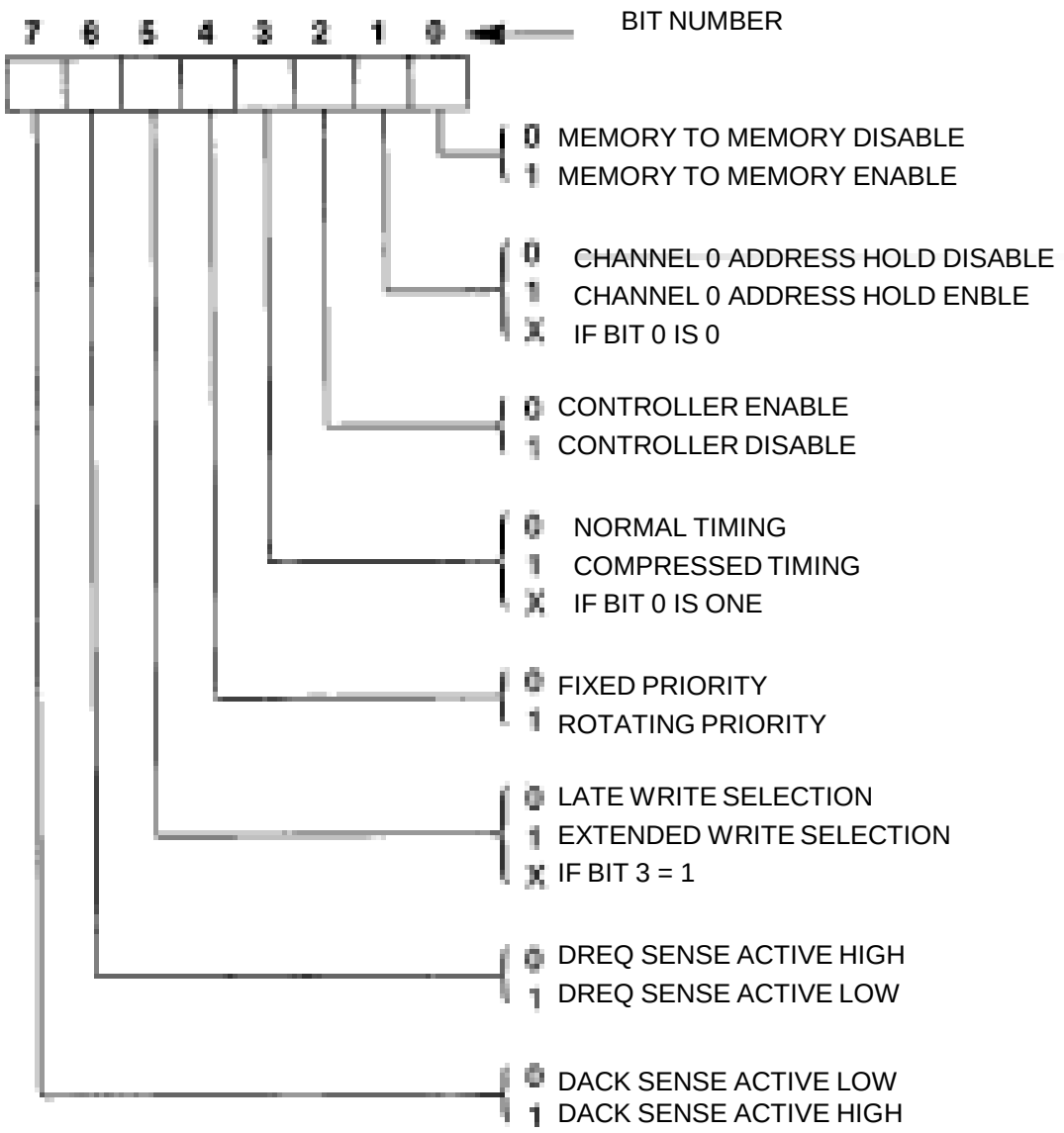
- When the peripheral is ready for the data transfer it sends a high signal to DRQ
- When the DRQ has been received and the channel enabled the control logic sets HRQ high.
- In the next cycle the MPU relinquishes the buses and sends the HLDA Signal to the 8237.
- After receiving the HLDA signal the DMA asserts AEN (address enable) signal high.
- When the entire address A15 –A0 is available on the address bus, the DMA send DACK to the peripheral



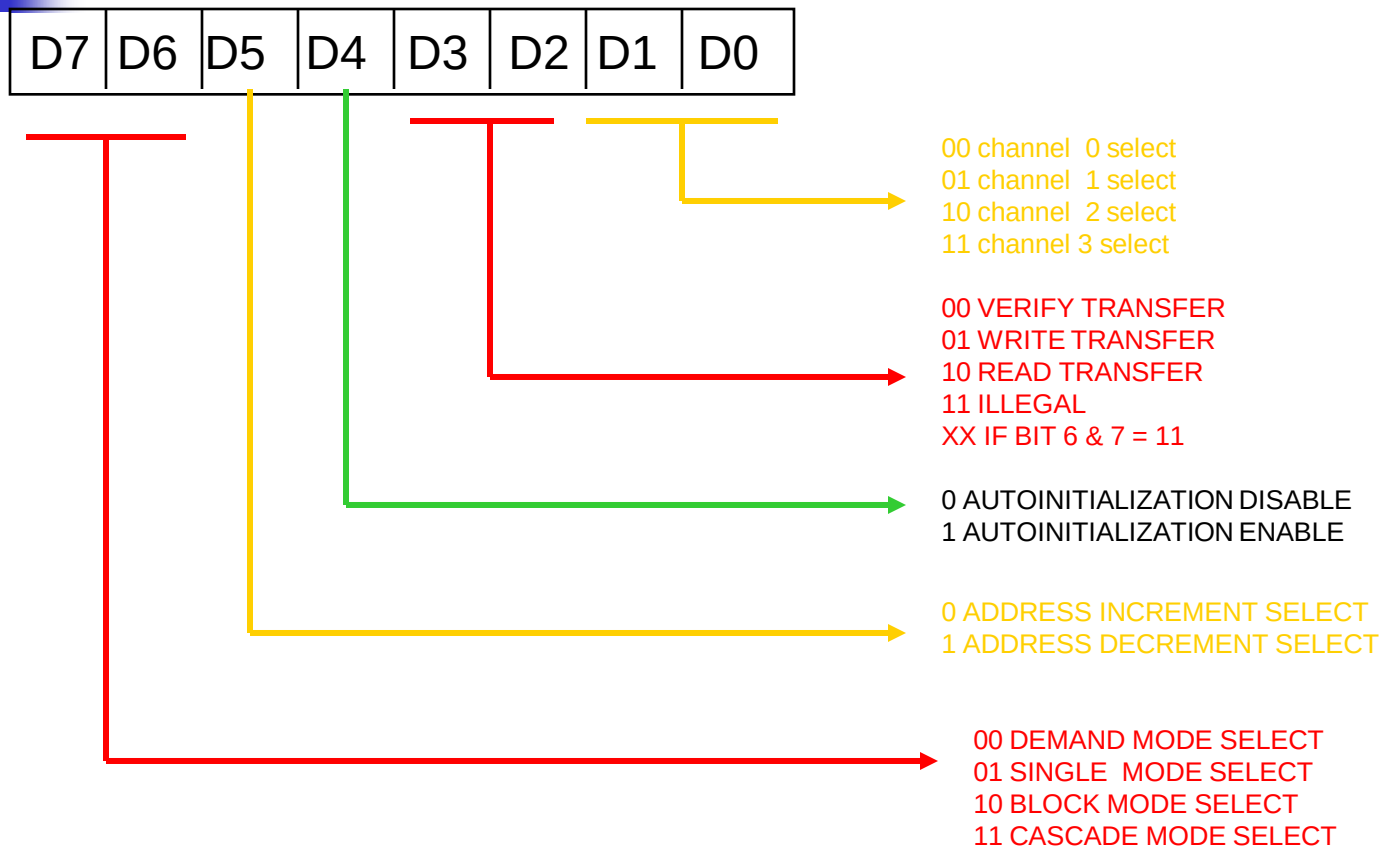
- The DMA controller continues the data transfer by asserting the necessary Control signals until DACK remains high.
- At the end of the data transfer the DMA asserts EOP (BAR) signal low that can be used to inform the peripheral that the data transfer is complete.the DMA data transfer can also be terminated by sending the low signal to EOP(BAR) from outside.


DECREMENTOR
TEMP WORD COUNT REG (16)
INC/DECREMENTOR
TEMP ADDRESS REG (16)
I/O BUFFER
A0-A3
16 BIT BUS
16 BIT BUS
READ BUFFER
BASE ADDRESS (16)
BASE WORD COUNT (16)
READ/WRITE BUFFER
CURRENT ADDRESS (16)
CURRENT WORD COUNT (16)
OUTPUT BUFFER
A4-A7
A8-A15
COMMAND CONTROL
EOP
RESET
CS
READY
CLOCK
AEN
ADSTB
MEMR
MEMW
IOR
IOW
TIMING AND CONTROL
WRITE BUFFER
READ BUFFER
D0-D1
DREQ0-DREQ3
4
HLDA
HRQ
DACK0-DACK3
4
PRIORITY ENCODER AND ROTATING PRIORITY LOGIC
COMMAND (8)
INTERNAL DATA BUS
I/O BUFFER
D80-D87
MASK (4)
READ WRITE MODE (4 x 6)
STATUS (8)
TEMPORARY (8)
REQUEST (4)

Command Register



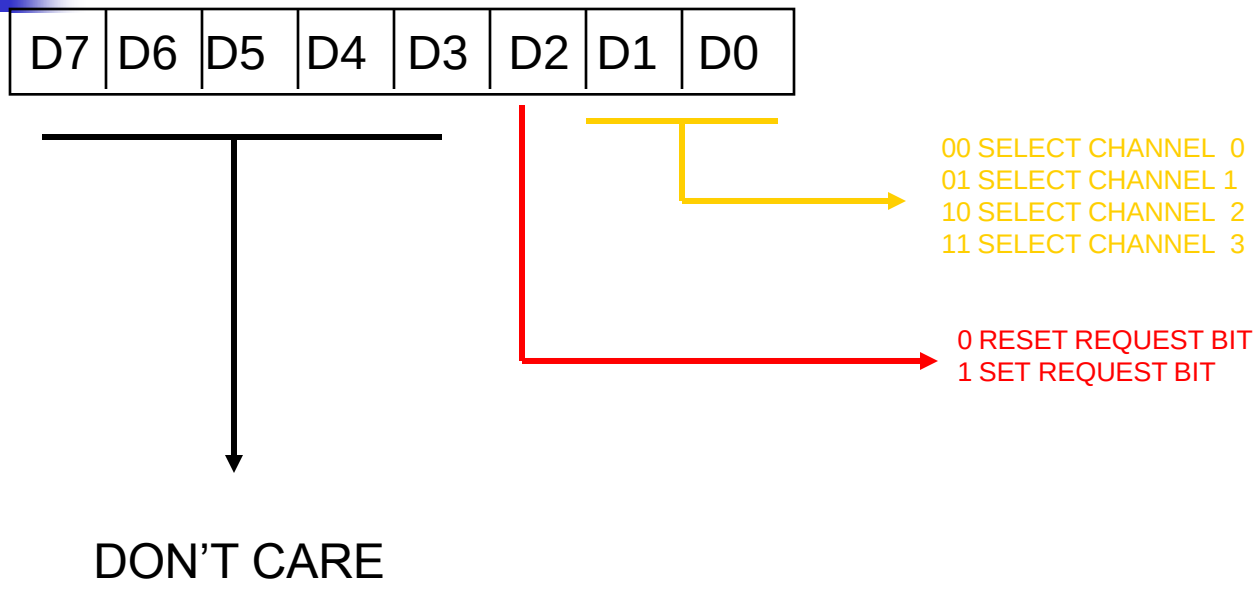
Mode Register



Modes of Operation

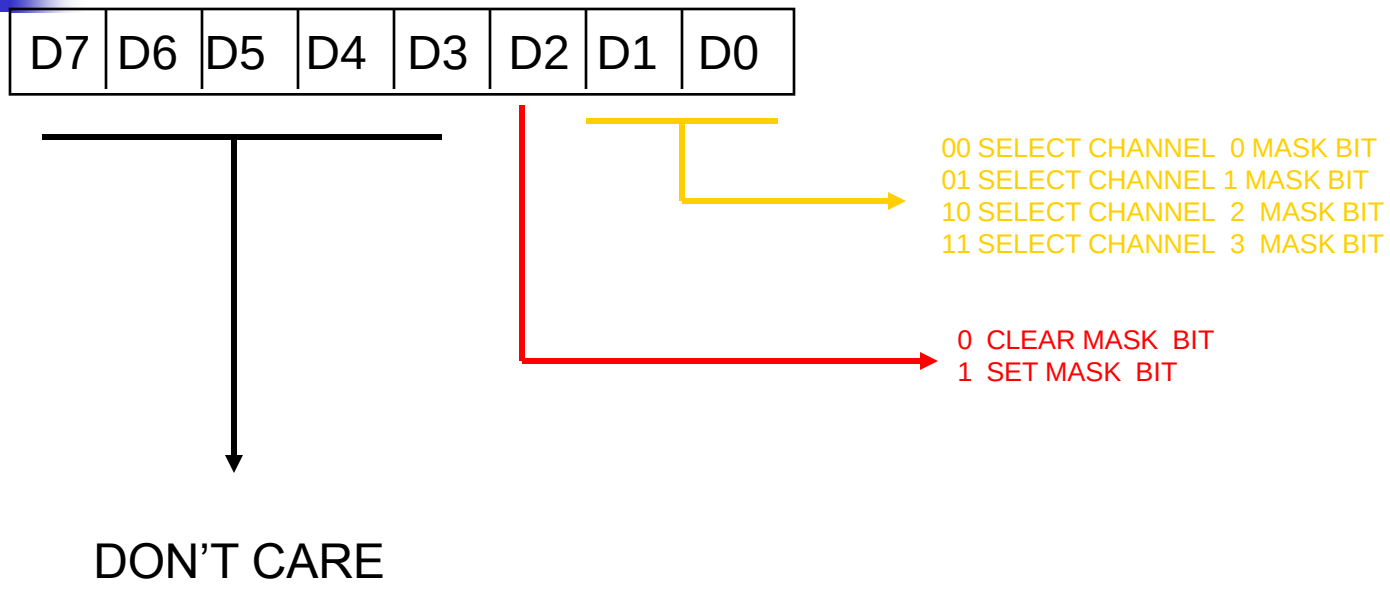
- Demand Mode
  - DMA continues until an external EOP is given or as long as DREQ input is active
- Single Mode
  - HOLD signal is withdrawn after one byte of transfer. If DREQ line continues to be active DMAC again requests for next byte transfer through HOLD request.
- Block Mode:
  - Block of data is transferred. Transfer is stopped when terminal count becomes zero
- Cascade Mode:
  - More than one 8237 are present in the system

Request Register

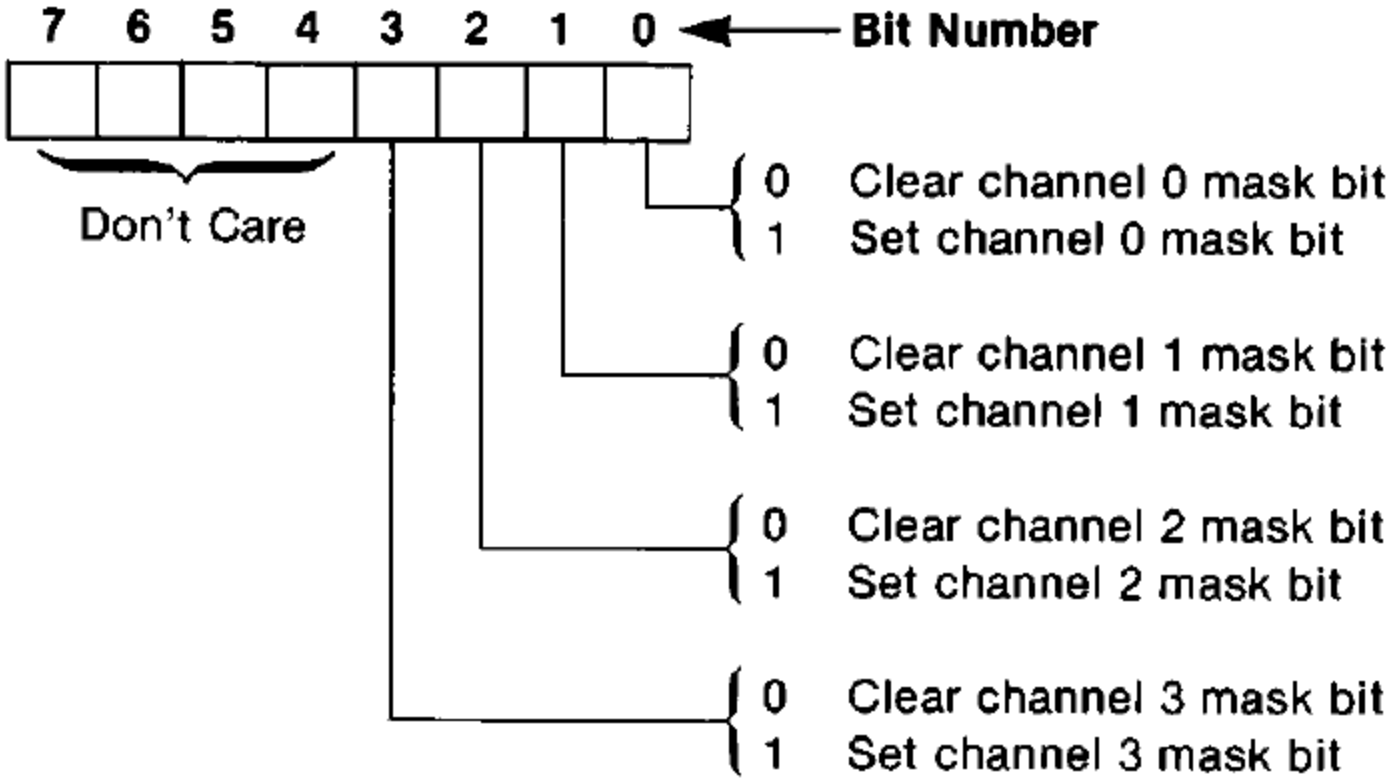


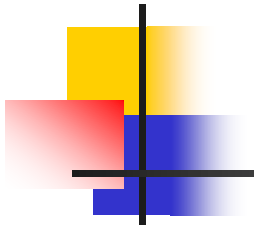
Mask Register

Mask Register



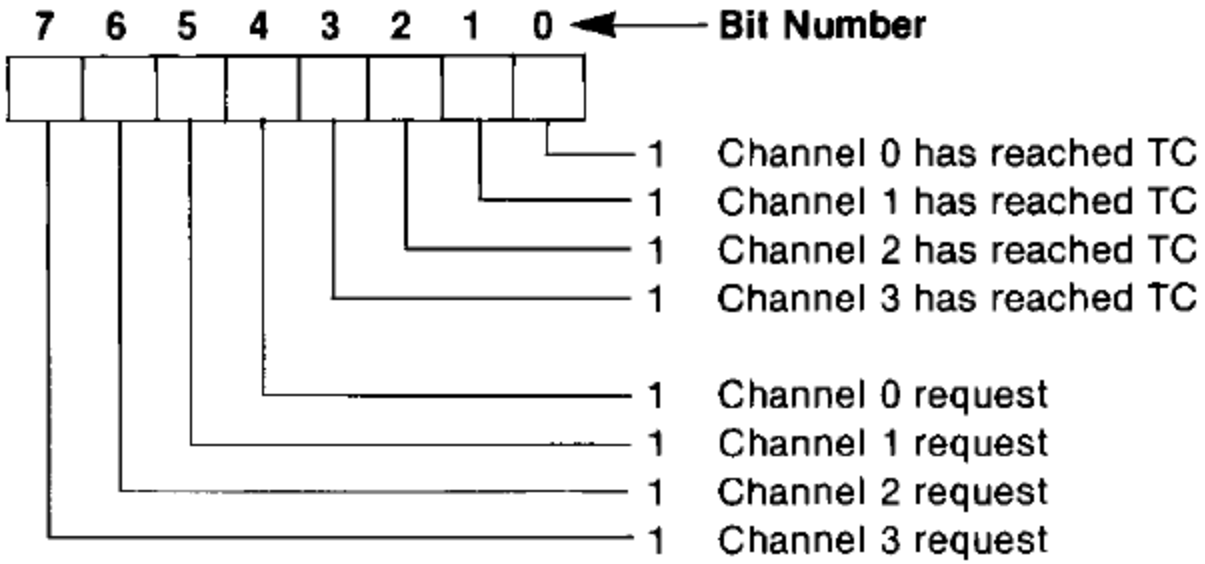
Alternate way of setting Mask Bits





Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Status Register



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